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GENERIC LINEAR MICROCIRCUIT TEST REQUIREMENTS

Boeing Aerospace & Electronics

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13. ABSTRACT (Maximum 200 words)

This is the final report for the Generic Linear Microcircuit Test Requirements Program performed for Rome Laboratory (formerly Rome Air Development Center). The objective of this program was to develop new series-4000 test specifications to standardize testing of linear devices. The drafts developed under contract will replace the existing series-4000 methods in MIL-STD-883C. New series-4000 drafts for 11 device families were developed, which will cover the majority of the linear microcircuits used in military systems. The test methods specified in each draft referenced a variety of sources including M38510 slash sheets, industry standard procedures, literature, existing test methods in MIL-STD-883C, and newly developed methods. Completion of these drafts will provide more consistent testing of linear devices. This report reviews all aspects of the program.

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PREFACE

This final report for the effort "Generic Linear Microcircuit Test Requirements" was prepared by Boeing Aerospace & Electronics, a division of the Boeing Company located in Seattle, Washington. Work was performed under contract # F30602-89-C-0169 for Rome Air Development Center (RADC) at Griffiss Air Force Base in New York, with Ms. Nancy Koziarz the RADC technical monitor. The period of performance for this contract was from August 1989 to September 1990.

This program was performed by the Parts Test and Applications group within the Electronics Systems Division of Boeing Aerospace & Electronics. The program manager was E. LeRoy Smith and the technical leader was Steve K. Tanemura. Significant contributions to the program were made by Ronald R. Mitchell, Dennis W. Nichol, M. George Motnyk, and Robert W. Deszell. The proposed generic test methods developed during this program and discussed in this report are a result of the diligent effort applied by this team.

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Note that each of the series-4000 test methods attached in appendix A include numerous test circuits, waveform diagrams, and test tables.

EVALUATION

This effort focused on updating and developing new linear test methods for inclusion into MIL-STD-883. The additional details in the new methods will allow manufacturers and users of the microcircuits to verify device performance by ensuring the same methods are used to measure the device. This effort was fully successful in identifying the required tests, minimal equipment, measurement accuracy/resolution, and procedures for 11 device families. The obsolete 4000 series contained in MIL-STD-883C will be replaced by the method developed during this effort.

The test methods which appear in the Appendix of this report will be placed into MIL-STD-883. They are published here for general information only. This is not a living document so any future changes will appear only in amendments or revisions to MIL-STD-883.

NANCY KOZIARZ

1.0 INTRODUCTION

This is the final report on the Generic Linear Microcircuit Test Requirements Program. This effort was initiated by RADC in August of 1989, and was completed after twelve months of technical work in August of 1990. Included in this report are all of the significant achievements and accomplishments of the effort.

The goal of the program was to develop standardized test methods that could be applied to a wide variety of linear device types. These test methods would be incorporated into MIL-STD-883C, replacing the old series-4000 test methods. This was necessary since the existing series-4000 methods were limited to testing operational amplifiers and used outdated/obsolete methodology. Also, the lack of standard methods forced manufacturers and other test facilities to develop test procedures for other types of linear devices on their own. This often lead to widely divergent test methods being used on the same type of device, which not surprisingly produced very different results. The development of these new methods would remedy this situation by giving test engineers a guide on which to base characterization and screening tests. This would result in more consistent testing of these critical linear devices.

As a result of this program, a total of 11 new series-4000 test methods were developed. These test methods cover 11 different linear families and thus cover a wide range of individual device types. In developing these test methods, much care was taken to ensure that they remained "generic" so that they could be implemented by any particular test facility. The steps taken to accomplish these tasks are described in the pertinent sections of this report.

This report is organized as follows:

Section 2	Program flow
Section 3	Selection of linear device families
Section 4	Parameter selection
Section 5	Test method development
Section 6	Test method preparation
Section 7	Overview of individual test methods
Section 8	Summary and conclusions
Appendix A	4000 Series Linear Test Methods

The Linear test methods included in appendix A are for information purposes only. The official methods will be contained in the next revision to MIL-STD-883C.

2.0 PROGRAM PLAN

The program plan used for this effort is shown in figure 2.0-1. To best carry out the objectives and goals of the contract, the work was broken into three main tasks:

1) Document Review and Parameter Selection
2) Test Method Development
3) Preparation of Test Method Specifications

The remainder of this section explains the rationale of the program plan and describes each of these tasks and their component subtasks in detail.

2.1 Program Rationale

To develop generic linear microcircuit test methods required us to take several factors into consideration. The large number of different linear device types commercially available meant that the finished test methods would have to cover a variety of device types. This required us to develop a philosophy which would allow the logical grouping of device types in a manner to ensure that linear microcircuits used by the military were covered, and to avoid developing literally hundreds of test methods and procedures. The wide variety of devices covered under each test method necessitated the development of flexible test procedures which could be adapted to several implementations of the same part type. Yet this need had to be balanced with the fact that the methods had to be detailed enough to ensure that different test laboratories using these methods could confidently compare data results without the fear of having incompatible data sets. Also, the test methods had to take into consideration that the numerous test laboratories that would use them had different test facilities. This placed increased importance on several critical test issues such as test equipment and test circuitry.

The program flow used in this effort was designed to satisfy these diverse needs. A comprehensive document review phase was included to ensure that all the major linear device families would be included in the new series-4000 test methods. During this review an extensive search and evaluation of existing and new test methods was also performed to identify all potential test procedures. These procedures could then be compared to determine the best choice for the series-4000 drafts. When developing the drafts, special attention was paid to addressing several critical test issues identified at the beginning of the program. To further ensure the flexibility and completeness of the drafts, a review by several linear device manufacturers and test facilities was also made. By following this plan we were able to confidently develop generic test procedures for all significant linear device families.

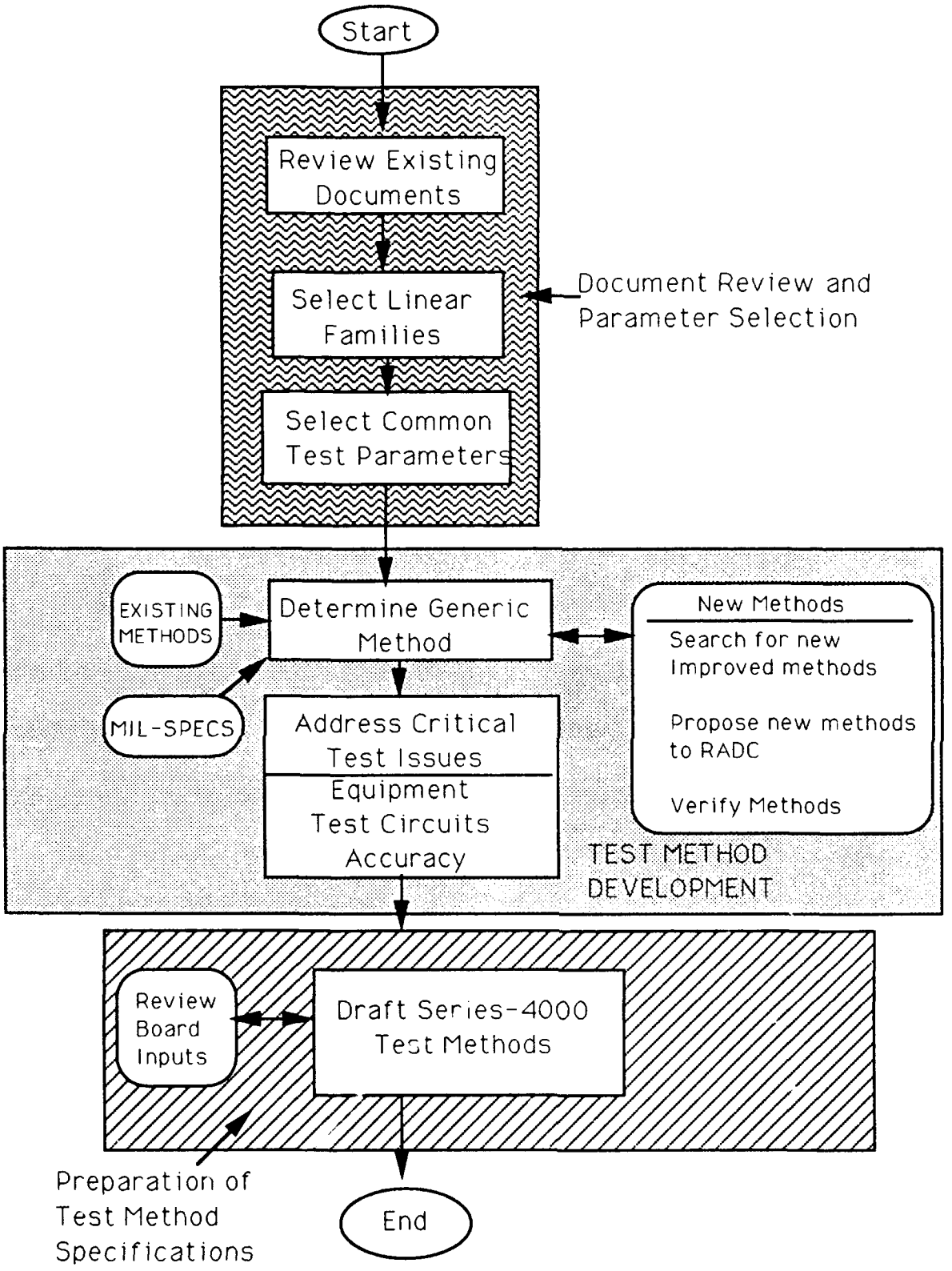


Figure 2.0.1 - Program Flow

2.2 Program Description

Figure 2.0-1 shows the basic program flow used in the contract. This section will give a more detailed description of each task shown in the flow chart.

Document Review and Parameter Selection: In this phase of the program, the basic information needed to perform the contract was obtained through a rigorous review of exisiting documents. This phase was divided into the following three subtasks.

Review Existing Documents: The purpose of this task was to obtain the information necessary to develop the generic test methods. The documents reviewed included military specifications, test literature/reports, and existing test documents.

Select Linear Families: At the start of the effort, an initial list of linear families to be covered by the test methods was submitted. Based on the information collected in the document review, this list was modified to reflect the current and expected military usage of these linear devices. This included the elimination, addition, or consolidation of device families.

Select Common Test Parameters: For each linear family, decisions were made on which parameters typically called out in the device specifications would be covered in the new series-4000 test methods. A selection philosophy was formulated and applied to each of the linear families previously identified. The final parameter lists were also reviewed by RADC for completeness.

Test Method Development: Once a decision was made on which parameters would be covered, work began on developing the test method to be specified in the series-4000 drafts. This phase consisted of two primary subtasks.

Determine Generic Method: In this step a generic test method was selected for each of the predetemined device parameters. This required the evaluation of several sources which included current military specifications, M38510 slash sheets, industry literature and new test methods. As seen, the use of new methods required approval from RADC and verification testing before being included in the series-4000 drafts.

Address Critical Test Issues: For each test method the critical test issues of test equipment, accuracy, and test circuitry had to be addressed. This was done to ensure that the methods could be easily implemented and still supply consistent results.

Preparation of Test Method Specifications: The final task of the program was the writing and preparation of the test methods for inclusion in MIL-STD-883C. These were drafted on a format based on the current series-4000 test methods. To ensure completeness

and applicability, the test methods were reviewed by several parties which included RADC and other linear device manufacturers.

The above program flow served the goals of the program by enabling us to efficiently develop the required generic test methods. By performing an in depth review phase at the outset of the program, we were able to quickly establish a framework on which to base each of the series-4000 test methods. Using this framework allowed us to develop complete test procedures that could be adapted to test a broad range of linear device types for application in military systems.

3.0 DEVICE FAMILY SELECTION

The first task performed in the document review phase was the selection of those linear families that would be covered by the new documents. Twelve different families were cited in the statement of work for this contract. These were:

1) Voltage Comparators
2) Operational Amplifiers
3) Data Converters
4) Voltage Regulators
5) Voltage References
6) Voltage-to-Frequency Converters
7) Line Drivers
8) Flash Data Converters
9) Analog Multipliers
10) Sample-and-Hold Amplifiers
11) Charge Coupled Devices
12) High-Power Devices

For each of these families, device specifications for one or more typical devices were examined. These specifications included MIL-M-38510 slash sheets, DESC drawings, Boeing Source Controlled Drawings (SCDs), and manufacturer data sheets. During this review it was discovered that an important linear family, analog switches, had been inadvertantly omitted from the initial list. Adding analog switches made a total of 13 linear families to be studied.

3.1 Selection Process

One of the first issues that had to be addressed in the program was to determine the areas of coverage for each of the new series-4000 drafts. Basically there were two logical formats for the test methods. One would be to base each test method on a specific family or type of linear device. For example, one method would be developed to cover voltage comparators, a second for analog multipliers, a third for data converters and so forth. The second possibility would be to develop test methods by parameter type. For example, one test method would cover input offset voltage, while a second measures line regulation, and other methods would be developed to cover the remaining parameters of interest.

While each choice could be feasibily implemented, we decided to base the test methods on linear families rather than individual parameters. This would lengthen the size of each test method since test procedures for several parameters would have to be included. However, the methods would also be easier to use since a test engineer developing a test for a voltage regulator would only need to reference one document rather than the 7 or 8 that would be needed if a parameter-based format was used. Also, since the majority of the parameters for a given family of

devices can be measured with a single test circuit, the amount of additional overhead needed to develop family-based test methods would not be significant.

Because of our choice to develop family-based test methods, one of the purposes of the document review was to ascertain the variety of device types that each method would have to cover. This would allow us to identify those cases where two or more families could be consolidated into a single method, or where a single family would require multiple test methods. In determining the final groupings for the new series-4000 methods the most important factor was test compatibility. Our goal was for each method to contain one generic test circuit/setup that could be applied to every device type covered by the method. This forced us to make some changes with the initial 13 linear families previously listed. These situations are discussed in more detail in the following paragraphs.

Data Converters: It was apparent that testing of data converters would require two test methods; one for analog-to-digital (A/D) converters and one for digital-to-analog (D/A) devices. The inclusion of a separate method for flash data converters was also retained since the high speeds of flash A/D devices would require completely different test methods from standard A/D converters.

Charge Coupled Devices: Our initial review of charge coupled devices (CCDs) showed a scarcity of such devices in the commercial market. Furthermore, those devices identified, performed a wide variety of different functions such as analog shift registers and photo transistor arrays. Because the number and functions of CCDs are few and scattered, developing generic methods specifically for CCDs would be a difficult task. Such a method would be forced to cover a wide variety of diverse parameters making it cumbersome to use and hardly generic in scope. Thus a distinct method for CCDs was deemed infeasible and dropped from consideration.

High Power Devices: This catagory of devices became redundent as our document review progressed. Those devices that were classified as "high power", functioned and had similar parameter sets to low power devices such as voltage regulators and references, and operational amplifiers. These parameters could be measured using the same techniques as low powered devices provided that the test engineer used equipment capable of generating and measuring the required high voltage or current signals. Test circuitry would also have to be designed to accept the higher amperage that would flow through the circuit. An additional factor that would require consideration would be thermal characteristics. While these concerns are certainly important, they represent device specific test problems that require the attention of the test engineer and not the development of new test procedures. Since the function of the so called "high power" devices cut across several device families, several parameters would be specified in two instances, once in

the high power device test method, and once in their functional linear family method. This ran counter to our philosophy of avoiding the development of multiple methods for a single type of parameter. For these reasons, a separate test method for High Power Devices was not developed in this effort.

Line Drivers: While line drivers have been classified as linear microcircuits, their operating characteristics more closely resemble digital devices. Typical line driver specifications list parameters normally associated with digital devices. Test setups to measure these parameters also resemble those used for digital microcircuits. Examining MIL-M-38510 slash sheets for line drivers shows that the series-3000 digital test methods are called out for each parameter. This effectively eliminates the need to develop a series-4000 linear test method since it is not the intent of this program to duplicate or change the series-3000 digital test methods. Because of this, line drivers were not included in the final list of linear device families.

3.2 Final Device Family Selection

Based on our document review and evaluation the original list of 12 linear device families was reduced to 11. These families cover the vast majority of linear devices used in military systems. list of the 11 families and a brief description of the types of devices included in each is provided in this section.

Analog-to-Digital Converters: Covers low-speed unipolar or bipolar A/D converters.

Digital-to-Analog Converters: Covers bipolar or unipolar D/A converters of up to 16-bits resolution. Test setup accomodates both voltage output and current output D/A converters.

Flash Converters: Covers those parameters for high-speed A/D flash converters that require the use of digital signal processing (DSP) measurement and analysis techniques.

Analog Multiplier: Covers both single-ended and differential input analog multipliers. Procedures can be applied to two quadrant and four quadrant multipliers.

Analog Switches: Covers single and multi switch devices with or without digital control inputs. Definitions cover both CMOS and JFET type switches.

Voltage Comparators: Covers voltage comparator integrated circuits. A successive approximation technique is included to test high-speed comparators not amenable to the standard nulling amplifier test method.

Operational Amplifiers: Covers operational amplifier circuits including those with low leakage currents.

Sample-and-Hold Amplifiers: Covers both sample-and-hold and track-and-hold amplifiers with internal or external hold capacitors. The procedures are applicable to inverting and noninverting amplifiers.

Voltage-to-Frequency Converters: Covers voltage-to-frequency integrated circuits.

Voltage References: Covers fixed and pin programmable voltage reference devices.

Voltage Regulators: Covers both positive and negative voltage regulators. Fixed and adjustable regulators are covered by the test procedures.

3.3 Summary

The initial list of linear device families was modified as a result of our in depth document review phase. Based on this review, a total of 11 linear families are represented in the new series-4000 test methods. We feel that these families cover the majority of linear devices used in military systems. Upon the completion of this task, the next phase of the program, parameter selection, began.

4.0 SELECT COMMON PARAMETERS

The next task to be completed after the selection of linear device families was to determine what parameters would be covered in each of the test methods. This required us to develop a criteria to determine what a generic parameter was, and to apply this to typical device specifications for each linear family. Once these parameters were determined, a decision was made on how to group them for test method development.

4.1 Initial Review

Much of the work in selecting parameters was performed during the initial document review. As previously mentioned, during this review we examined several device specifications for each linear family of interest to the program. An additional benefit of this review was that it allowed us to see what kind of parameters were called out by typical linear device specifications in each family. For each of the specifications examined, a list of the parameters called out for measurement was made. This was tabulated in the form of a matrix showing how often each parameter was called out amongst all of the specifications examined. An example of one of these matrices is shown in figure 4.1-1.

At the completion of the document review, a matrix existed for each of the device families listed in the original statement of work. Some of these matrices were later discarded when particular linear families were dropped from the program (as discussed in section 3). However the remaining matrices were then used to aid us in the selection of parameters to be included in the new test methods.

4.2 Selection Philosophy and Criteria

The basic philsophy used for parameter selection was to examine each parameter and see how often it was marked in the matrix. Those parameters marked in the majority of the columns were strong candidates for selection. Those listed in only 1 or 2 cases would most likely be classed as 'device specific' parameters and thus would not be good candidates for inclusion. In all cases parameters called out for MIL-M-38510 devices received more weight than parameters listed in commercial specifications.

For some part families, such as operational amplifiers (figure 4.1-1), the choices were rather easy since all of the device specifications examined called out mostly the same parameters. In other cases however, the decisions required more thought. The voltage regulator matrix shown in figure 4.2-1 appears to have some parameters that should not be included. Closer examination reveals that this is caused by the different parameters called out by fixed regulators and adjustable regulators. Since any test method developed for voltage regulators must include both

Operational Amplifier					
	Part Number			TA = + / - 25 DEG C	
Parameters	M38510/135 Device 05 (1)	M38510/122 Device 04 (2)	M38510/114 Device 05 (3)	M38510/119 Device 05 (4)	M38510/101 Device 04 (5)
VIO	X	X	X	X	X
IIB	X	X	X	X	X
IIO	X	X	X	X	X
PSRR	X	X	X	X	X
CMRR	X	X	X	X	X
VIO (adj.)	X	X	X	X	
IOS	X	X	X	X	X
ICC	X	X	X	X	X
VOP	X	X	X	X	X
AVS	X	X	X	X	X
SR	X	X	X	X	X
ts		X	X	X	X
TR(tr)		X	X	X	X

Description/Notes:

(1) Internally compensated ultra low noise, broadband, generic number OP-37A.

(2) Single operational amplifier, internally compensated, precision, high slew rate, generic number 2500; other parameters not listed are: Vout.

(3) JFET operational amplifier, high performance, wide band, low offset, generic number L156A.

(4) BI-FET dual operational amplifier, generic number LF153; other parameters not listed are: CS, NI(BB), NI(PC).

(5) Single operational amplifier, externally compensated, generic number LM747A; other parameters not listed are: CS, NI(BB), NI(PC)

(6) "X": indicates parameter called out in device specification.

Figure 4.1-1 Operational Amplifier Matrix

Voltage Regular					
	Part Number		TA = +/ -25DEG C		
Parameters	M38510/107 Device 01 (1)	M38510/117 Device 03 (2)	M38510/102 Device 01 (3)	M5962-87675 Device 02 (4)	M38510/115 Device 08 (5)
VOUT	X	X			X
VRLINE	X	X	X	X	X
VRLOAD	X	X	X	X	X
ISCD	X		X		X
IOS	X	X	X		X
VSTART	X	X			X
VRTH		X			X
IADJ		X		X	
VREF			X	X	
IMIN		X	X	X	

DESCRIPTION/NOTES:

(1) Fixed positive voltage regulator (+5V @ 1.5amps max), generic number LM109.

(2) 3-terminal adjustable regulator (1.25V<Vo<37V @ 0.5A), generic number LM117H; other parameters not listed are: VOUT(recov).

(3) Adjustable precision poltage regulator, generic number LM723; other parameters not listed are: VZ.

(4) Adjustable 3A positive voltage regulator (-24V @ 1.0A), generic number 7942; other parameters not listed are: Ipk.

(5) Fixed voltage regulator (-24V @ 1.0A), generic number 7924; other parameters not listed are Ipk

(6) "X" indicates parameter called out in device specification.

Figure 4.2-1 Voltage Regulator Matrix

types of devices, nearly all of these parameters were eventually included in the voltage regulator test method. A more extreme example is the analog multiplier matrix shown in figure 4.2-2. In this matrix there appears to be little consensus in which parameters should be included in the generic test method. For this case, we placed an emphasis on covering the parameters called out by the JAN devices. Thus for analog multipliers we chose to include those parameters specified by the M38510/139 device listed in column 1. This approach was taken because the purpose of the new series-4000 test methods is to define standard methods to test military (JAN) devices. Thus it only makes sense to ensure that the test methods cover the basic parameters specified by JAN devices in the M38510 slash sheets.

Each matrix was examined in a similar manner. As a result of this examination, we were able to identify four different types of parameters. These four catagories were: (1) Device specific parameters not suited for generic treatment; (2) Parameters which could be measured using the existing series-3000 digital test methods; (3) Parameters covered by existing series-4000 test methods; and (4) Parameters requiring new test methods to be developed. Our stance regarding each of these catagories is provided in the following paragraphs.

Device Specific Parameters: Device specific parameters were defined as those listed in only a small number of the device specifications examined in the initial review. These parameters were not selected for inclusion in the new series-4000 test methods. Typically they were special parameters included by the manufacturer to check that special functions or circuitry operated correctly. Adding these parameters would simply add clutter and make the new series-4000 methods unwieldy to use. Since the purpose of the contract was to develop generic methods to test linear devices, it was not appropriate to add numerous test procedures and special circuits to measure esoteric or seldomly used parameters.

Digital Parameters: While the emphasis of this effort was on linear test methods, we identified several parameters common to linear devices that could be measured using the series-3000 digital test methods. For some device families (such as data converters) these parameters existed due to the digital component of the devices; for others it was simply the fact that they are defined the same for linear and digital devices. Figure 4.2-3 lists a table of those parameters that can be measured using series-3000 methods. Since these parameters are all commonly called out, they could not be ignored and left out of the new series-4000 test methods. It was decided to include these parameters in the new test methods, but to reference the series-3000 test method as the proper measurement technique.

Existing Series-4000 Parameters: The existing series-4000 test methods cover some of the parameters called out by operational amplifier military specifications. However, they are also

Analog Multipliers					
Part Number			TA = + / - 25 DEG C		
Para-meter	M38510/139 Device 04 (1)	280-22061 Device 101 (2)	5962-88733 Device 03 (3)	AD539 MIL-STD-883 (4)	MPY100 MIL-STD-883 (5)
VIO	X			X	X
IIB	X				X
IOS	X	X	X		
ICC	X	X	X		
SR	X				X
FT	X			X	X
AE	X			X	
NL	X				X
VOH		X	X		
VOL		X	X		
II		X	X		
IOUT				X	X
ROUT				X	X

Description/Notes:

(1) 4 quadrant analog multiplier 4%, generic number 4213; other parameters not listed are: MA, IIO, CMRR, VOP, PSRR.

(2) 6-bit binary rate multiplier, generic number 5497; other parameters not listed are: VIC, IIH, IIL.

(3) 16X16 bit multiplier accumulator, generic number 7C510; other parameters not listed are: IOZ.

(4) Wideband dual-channel multiplier/divider, ANALOG DEVICES, generic number AD539; other paramters not listed are: PSRR, IO(pk), IO(offset).

(5) Multiplier-driver, BURR-BROWN, generic number MPY100; other parameters not listed are: VIN(range), VOUT, IQ, RIN.

(6) "X" indicats parameter called out in device specification.

Figure 4.2-2 Analog Multiplier Matrix

Device Family	Parameter
Analog Multiplier	Power Supply Current Output Short Circuit Current
Analog Switch	Power Supply Current Voltage Output Low Voltage Output High Input Leakage Current Propagation Delay
A/D Converter	Power Supply Current Input Leakage Current Output Leakage Current Output Short Circuit Current Voltage Output Low Voltage Output High
Comparators	Power Supply Current
D/A Converters	Power Supply Current Input Leakage Current
Operational Amplifier	Power Supply Current Output Short Circuit Current
S/H Amplifier	Power Supply Current Input Leakage Current
Voltage Reference	Output Short Circuit Current
Voltage Regulator	Output Short Circuit Current
Voltage-to-Frequency Converter	Power Supply Current Voltage Output Low

Figure 4.2-3 Parameters Using Series-3000 Digital Test Methods

obsolete and are not in a format compatible with that chosen for the new series-4000 methods (being grouped by parameters rather than linear families). It soon became apparent that the best choice would be to eliminate the existing series-4000 methods rather than preserving them in some form so they could be called out in a manner similar to the series-3000 methods described above.

New Parameters: Since generic test methods for these parameters did not exist, these had to be covered by the new series-4000 methods. The majority of the parameters identified fell into this catagory.

4.3 Final Selection

The outcome of the matrix evaluation was a list of parameters for each device family that should be included in the new test methods. As a final exercise, we took the list for each linear family and checked that measuring all of the parameters on the list would result in a reasonably complete evaluation for a range of typical devices in the family. In some cases we found that this was not the case and some additional parameters were added. Typically this occurred in situations where parameters had to be added to cover an important subgroup of devices within a linear family (similar to the case involving voltage regulators discussed previously).

4.4 Parameter Groupings

The final decision that had to be made was in the groupings of the parameters for each of the test methods. The final lists for each linear device family primarily concentrated on static parameters. This was because the dynamic and timing parameters for most device types were not specified in a consistent manner. Only the parameter lists for the D/A converter and operational amplifier families had a significant number of dynamic parameters included on it. Because of this situation, it was decided to develop two series-4000 test methods for each of these families. One would specify static parameters, while the second would be used for dynamic parameters. This approach was chosen because the dynamic parameters would require different test circuits and equipment and thus could stand by themselves as individual test methods. For the remaining families, either no dynamic parameters were on the final parameter list, or those that were could be easily tested on the static parameter test circuit. Thus the total number of new series-4000 test methods grew from 11 to 13.

During the review phase with RADC some concerns were raised on whether this was the best approach. The scarcity of dynamic parameters proved troublesome in that it raised questions on whether the test methods would truly provide all the necessary information to perform a complete test on a linear device. To alleviate this concern, it was suggested that several dynamic

parameters required by M38510 devices be added to the appropriate test methods. This however, raised another problem on parameter groupings. Using our initial philosophy, we would be required to develop additional series-4000 test methods to cover the added dynamic parameters. This could result in a maximum of 22 test methods (two for each of the 11 linear families). This was clearly too many and thus a decision was made to return to the one test method per linear device family view. This required a total of 11 new test methods to be developed.

Once final parameter groupings were determined. Work began on the most important phase of the program, test method development.

5.0 TEST METHOD DEVELOPMENT

This section describes the process of selection and development of the generic test methods after the electrical parameters for each family had been identified. After reviewing several sources of test methods and identifying candidate methods, the first development step was to select a preferred test approach for each parameter. We then developed one or more generic test circuits to perform all the tests for a family. Next, we specified the test equipment required to perform the measurements. A critical problem at this stage was specifying the accuracy and resolution of the test equipment in a manner that would accommodate a wide range of performance within a generic family without overly restricting the choice of instruments.

5.1 Test Method Identification

After identifying generic electrical parameters for each family, we collected information on test procedures for measuring these parameters from a variety of sources. Selection criteria were applied to this set of possible test procedures to determine those most appropriate for development as generic series-4000 test methods. The methods thus identified were then carefully developed to make them applicable to testing all of the family members reviewed in the study. Since these parts are typical of those used in military systems, the test methods should serve for the majority of parts covered by the family description.

Our review of test methods covered four areas:

1. Existing series-4000 test methods were evaluated to ascertain which might be carried over to the new specification with possible revision and modification.

2. Digital test requirements for devices combining both analog and digital functions were examined and compared with test methods specified in MIL-STD-883 series-3000 test methods.

3. Established test methods for every family of devices were reviewed. Established methods included methods outlined in 38510 slash sheets, technical reports, manufacturers' data books, textbooks, ATE system literature, and our own experience in testing linear devices.

4. Newer methods dictated by advances in device performance levels or made attractive by advances in instrumentation or computer processing power were evaluated and tested in our laboratory.

The review and selection process for each area is discussed in detail in the following subsections.

5.1.1 Existing Series-4000 Parameters

The MIL-STD-883C section headed "electrical tests (linear)" consists of methods 4001 through 4007. The family of devices addressed by these tests is identified variously as "linear amplifier with differential inputs", "linear amplifier", "amplifier" or not at all. The device parameters covered by methods 4001 to 4007 are:

4001 - input bias current, input offset current, voltage offset

4002 - phase margin, slew rate

4003 - common mode input voltage range, common mode rejection ratio, supply voltage rejection ratio

4004 - gain, bandwidth, distortion, dynamic range and input impedance

4005 - power dissipation, output impedance

4006 - power gain, noise figure

4007 - automatic gain control range

The description "linear differential amplifier" is broader than the generic families identified in this program. It applies at least to operational amplifiers, sample-and-hold amplifiers, analog multipliers and voltage comparators. These series-4000 methods are called out for the named parameters in many of the MIL-M-38510 slash sheet group A electrical inspection tests. However, the test circuits and methods given in the slash sheets differ significantly in almost every case.

Our review of the original series-4000 linear test methods led us to conclude that the orientation was towards the specification of operational amplifiers as building blocks for small signal linear amplifiers. Performance in this application depends significantly on external compensating components and closed loop gain. Therefore, some parameters, such as power gain, automatic gain control range, bandwidth and input impedance, did not come through our selection process for generic parameters. Tests to assure such performance should be included within a procurement document rather than specified in a generic test method.

In summary, the existing series-4000 methods fell into two categories: those which covered parameters called out for test in the slash sheets but which differed significantly from the method required by the slash sheet, and those which were not called out in the slash sheets at all. Neither of these catagories were in line with our philosophy on test method development. Because of this, none of the existing series-4000 test methods were carried over in the the new test methods developed under this contract.

5.1.2 Series-3000 Test Methods

The possible usage of the series-3000 digital test methods in MIL-STD-883C occurred in two cases. The first involved those linear device types that also had digital functions built in. For these device types, several important digital parameters were specified. In other cases, the measurement technique for some parameters specified for linear devices did not differ from similar measurements made on digital devices. Examples of these parameters would be power supply current measurements, and output short circuit current tests. In both cases, the series-3000 digital test methods could adequately make the measurement. For these situations we decided not to write redundant test procedures to include in the series-4000 methods. Developing such procedures would lengthen the test methods and also make the test circuits more complicated due to additional equipment requirements. Instead, the appropriate digital test method was called out for each parameter.

5.1.3 Established Test Methods

The primary source for the generic test methods developed in this program was MIL-M-38510 specifications for linear integrated circuits. With the exception of flash converters, all the device families covered are mature linear integrated circuits. Each family is represented by one or more slash sheets which include test circuits, supporting notes, and tables of switch settings which together constitute a set of test procedures. We found that the separate slash sheets adopted a consistent method for measurement of the parameters selected for each family although the details of test circuits varied. Moreover, these methods were similar to the approaches utilized in our Teradyne A312 tester and described in the data books, technical reports and texts consulted in this effort.

An exception was the slash sheet approach to testing voltage comparator static parameters. In existing MIL-M-38510 slash sheets, voltage comparators are treated as operational amplifiers and tested with the output biased into the linear region. While this method has been used successfully for testing the older parts specified in the slash sheets, it may not suffice for the newer parts having very high voltage gain and non-linear transfer characteristics. A more generic test approach which would apply to both older parts and high gain devices is implemented in the Teradyne A312 tester. This approach is based on the functional definition of a comparator as a device having two discrete output states and would apply universally. We therefore based the generic test method on this approach while retaining the operational amplifier approach as an alternative method.

5.1.4 New Test Methods

'New' test methods were defined as procedures not documented in MIL-STD-883C or MIL-M-38510 slash sheets, or established as industry standards. Such methods may not actually be 'new' in the sense that they were initially developed under this contract, but could be alternate test procedures or improvements on existing methods to take into account the advances in device performance. Another possibility would be the use of an established technique in an area that it is currently not used. These would all classify as 'new' methods in the context of this contract.

A contract requirement was that any proposed new methods would be evaluated by Boeing after submittal to RADC. This evaluation would verify that the method operated correctly, and determine the benefits (if any) of the new method. For a new method to deserve consideration, definite improvements over existing methods in key areas had to be realized. These key areas included accuracy, reduction of test time, reproducability, and ease of implementation. Such improvements had to be distinct since our basic philosophy was not to include new methods unless they offered clear advantages.

During the course of the contract, two 'new' methods were included in the test methods. These were the integrating capacitor method for measuring low leakage currents on operational amplifiers, and the use of digital signal processing techniques for the measurement of dynamic performance of flash data converters. These methods will be described in more detail in the following sections.

5.1.4.1 Integrating Capacitor Method

The measurement of leakage currents such as input bias currents and input offset current is becoming increasingly difficult for state-of-the-art devices since many of them make use of field effect transistors or very low leakage current transistors as input devices. The standard method for measuring these currents uses voltage drops across resistors in the input circuit to the device to make these measurements. However, for very small leakage current, very large resistances are required which can produce noise and other instabilities. As an alternative, an electometer could be switched in to the device inputs. Unfortunately, these instruments are not always available in automatic test equipment and require carefully shielded input connections and relatively long instrument settling times. Another alternative is the Intergated Capacitor test method which requires only a simple circuit to accurately measure extremely small currents. This method was proposed for inclusion in the operational amplifier and comparator test methods.

Method Description: The Integrated Capacitor (ICap) test method makes current measurements by collecting charge on a capacitor.

For a given capacitor, the stored voltage can be calculated using the equation:

$$V = \frac{Q}{C}$$

where Q = (current)*(time)
C = value of capacitor

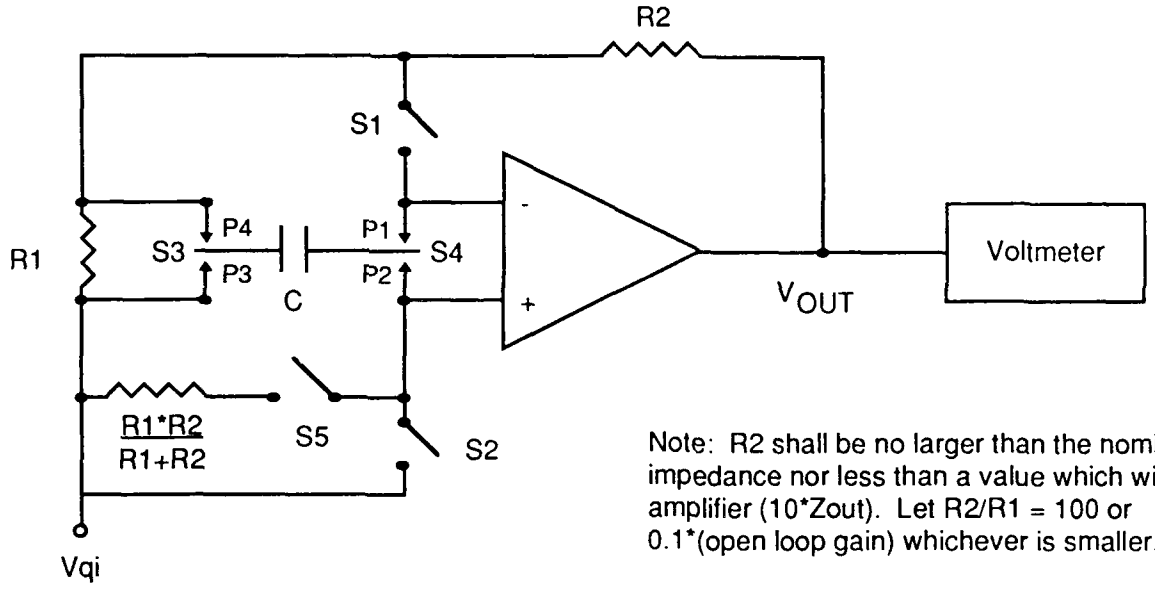
solving for the current, I_L and taking into account the passage of time between voltage measurements, we get:

$$I_L = \frac{(C)*(\Delta V)}{\Delta T}$$

The basic procedure used for the ICap method is to switch the capacitor to the positive or negative input pins of the amplifier under test in a feedback circuit (see figure 5.1.4.1-1). Voltages are measured at the output terminal by a standard voltmeter. The advantage of using this method is that instead of measuring the very small current, we are measuring the relatively large voltage at precise time intervals. This is a considerably easier measurement to perform. The ICap method can be used to measure input offset current, input bias current, and input offset voltage. It is also easy to setup, requiring only a few simple components. Figure 5.1.4.1-1 shows a schematic of the required test circuit and the equations used to measure each parameter.

Care should be taken in the choice of components to be used. In particular the switches should have isolation resistances in the neighborhood of 10,000 MΩ, and the storage capacitor should have a dielectric resistance of 400,000 MΩ.

Verification: To verify the accuracy and improvements gained by the ICap method, the following test procedure was used. A sample test device would be chosen and subjected to three measurements, one using the ICap method, one using the standard technique of measuring voltage drops across resistors, (also controlled by the Teradyne A312 ATE) and the last using a Keithly 485 Picoammeter. A special test interface adapter card was designed and fabricated for use with the Teradyne A312. This test circuit used the standard nulling amplifier apporach to measure operational amplifier parameters and is shown in figure 5.1.4.1-2. This adapter card was also modified to allow the picoammeter to be directly plugged into the circuit to make current measurements. Since the ICap circuit was designed to use the A312 as a controller, all tests would use the same basic fixture which would lessen the effects caused by external factors such as test sockets and wiring. The operational amplifier chosen for these tests was a Precision Monolithics Op 15A. The integrating capacitor used was a Component Research 0.01 μF low leakage, ultra stable capacitor.



Note: R2 shall be no larger than the nominal input impedance nor less than a value which will load the amplifier (10*Zout). Let R2/R1 = 100 or 0.1*(open loop gain) whichever is smaller.

Equations

$$V_{IO} = \frac{R1}{R2} * (V_{OUT} - V_{qi})$$

S1 = Closed, S2 = Open, S3 at P4, S4 at P1, S5 = closed

$$IL+ = \frac{C\,(V_{OUT}(B) - V_{OUT}(A))}{t_2 - t_1} * \frac{R1}{R2}$$

S1 = Closed, S2 = Closed, S3 at P3, S4 at P2, S5 = Open

Open S2, measure $V_{OUT} = V_{OUT}(A)$ after t_1 seconds
measure $V_{OUT} = V_{OUT}(B)$ after t_2 seconds

$$IL- = \frac{C\,(V_{OUT}(D) - V_{OUT}(C))}{t_2 - t_1} * \frac{R1}{R2}$$

S1 = Closed, S2 = Closed, S3 at P4, S4 at P1, S5 = Open

Open S1, measure $V_{OUT} = V_{OUT}(C)$ after t_1 seconds
measure $V_{OUT} = V_{OUT}(D)$ after t_2 seconds

$$I_{IB} = \frac{|IL+| + |IL-|}{2}$$

$$I_{IO} = |IL+| - |IL-|$$

Figure 5.1.4.1-1. Circuit Diagram and Equations For Integrating Capacitor Test Method

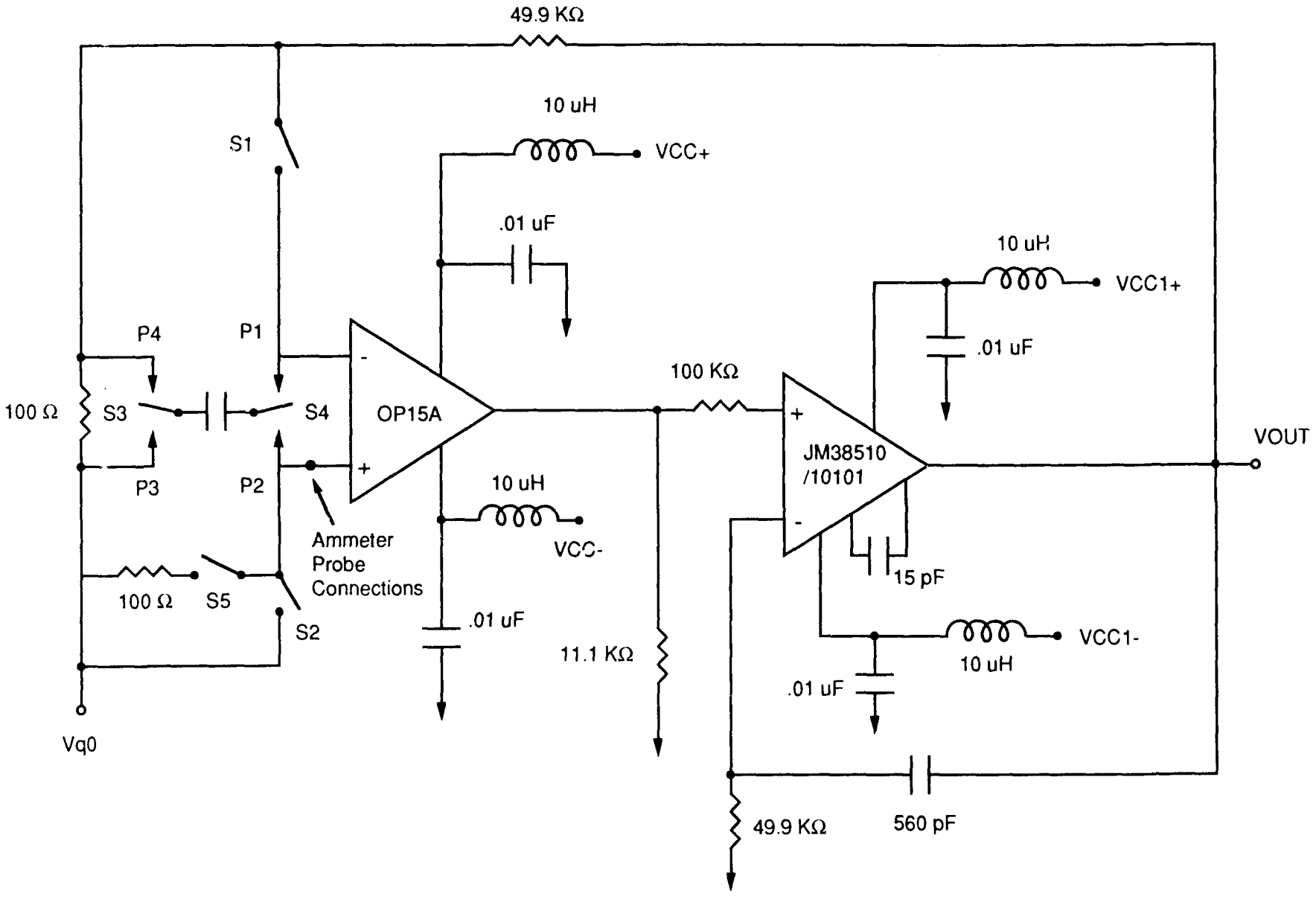


Figure 5.1.4.1-2 Teradyne A312 Test Setup For Integrating Capacitor Method

Testing using the ICap method was performed first using the Teradyne A312 hardware. A flow chart of the test program section for measuring the leakage current from the input of the negative terminal to the Op 15A is given in figure 5.1.4.1-3. Test results for this method were:

$$IL+ = 25.9 \pm 0.6 \text{ pA}$$
$$IL- = 9.4 \pm 0.3 \text{ pA}$$

The difference between IL+ and IL- was surprising but repeated measurements using different values for ΔT showed that these values were consistent. The probable cause for this variance is with switches S3 and S4 in figure 5.1.4.1-2. Since current from each input terminal passes through a different set of contacts, extra leakage can be added or cancelled from the current flowing into the capacitor when measuring IL+ and IL-.

Testing was also performed using the standard leakage current test method outlined in MIL-STD-883C. Like the ICap method, this method measures voltages instead of the small currents. Two measurements of input offset voltage (V_{IO}) are made. The first is made with the amplifier in a standard test configuration, and the second is made using the same circuit with a very large resistor connected to the input terminal (this is possible by replacing the capacitor in figure 5.1.4.1-2 with a resistor and setting the switched to the proper setting). Leakage current is then derived from the equation:

$$IL = \frac{\Delta V_{IO}}{R}$$

Unfortunately there are some inherent problems with this setup. If the value of 'R' is too small, the voltage drop across the resistor will have little effect and ΔV_{IO} will approach the resolution of the voltmeter used to make the measurement. Selecting a very large 'R' has the problem that the choice of precision resistors in the 10 MΩ+ range is limited, and such large resistors have the tendency to produce spurious noise. For the OP 15A, our Teradyne A312 setup used a 10 MΩ resistor which should result in a ΔV_{IO} of approximately 150 μV. Unfortunately the best resolution on the A312 voltmeter is 100 μV. Thus it is obvious that the voltage measurements will have considerable round off error, and any current values will similarly be suspect. Using this method on the A312 gave current values of either 0 pA, 10 pA or 20 pA, which is clearly inadequate.

The final test used a Keithly 485 picoammeter. The A312 test adapter was also used for this measurement, but in a bench top setting rather than one controlled by the A312. The ammeter was

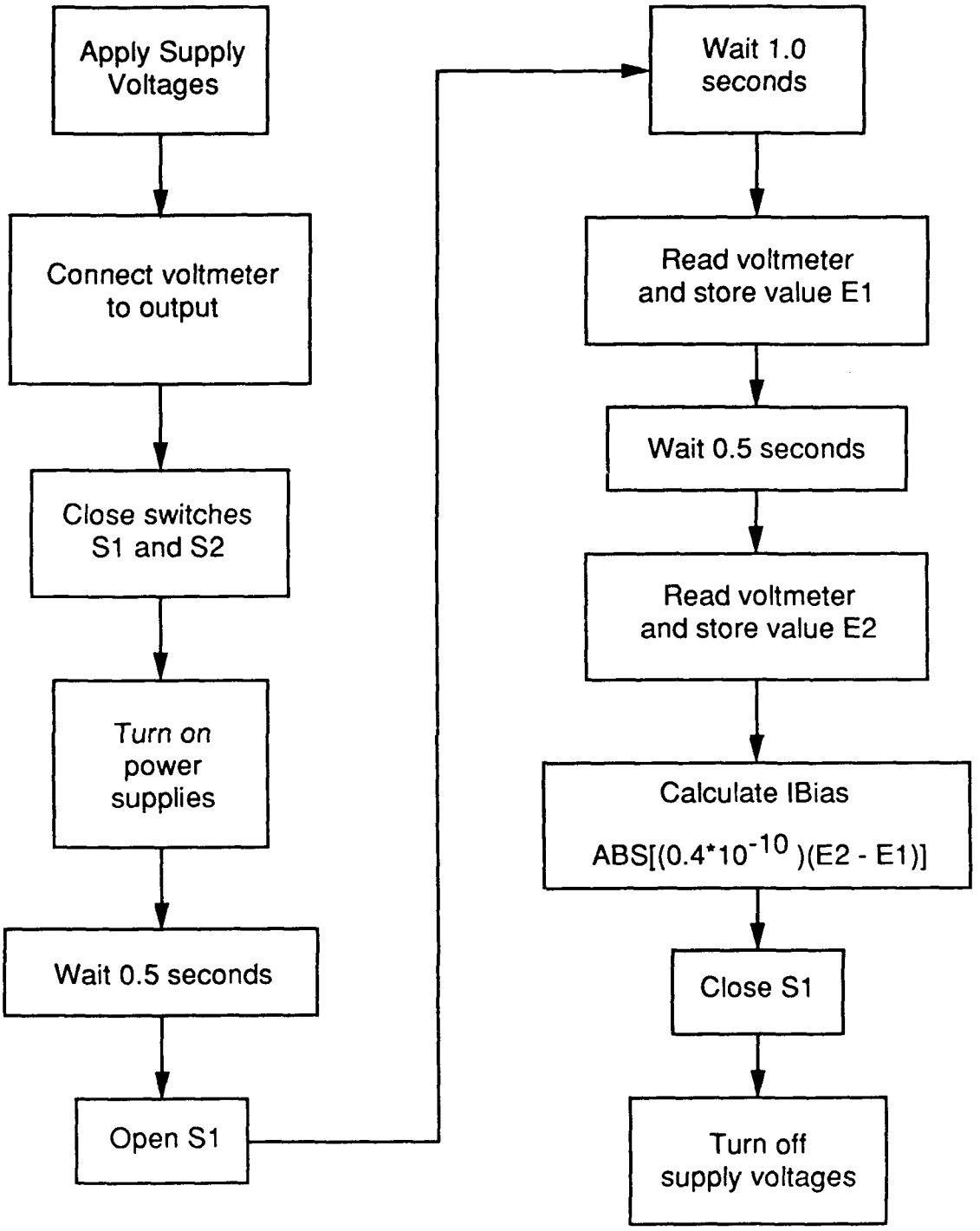


Figure 5.1.4.1-3 Flow chart for measuring bias current to negative input using Integrated Capacitor test method

directly plugged into the fixture via some special terminals, and the current in the input leads measured. Typical values were:

IL+ = 3.6 pA
IL- = 3.5 pA

These values were also measured several times and proved to be very consistent if sufficient settling time was allowed.

Analysis: The final results for the verification tests were not as good as anticipated. Leakage currents measured using the ICap method were the same order of magnitude as those measured using the Keithly Picoammeter, but differences did exist. However using the ICap method did allow for significant improvement over the method currently outlined in MIL-STD-883C.

Several possible factors could be responsible for the differences between the two sets of measurements. Measuring such low currents is always a difficult chore and a number of outside factors can influence the measurement by a few picoamps (which is significant when measuring currents < 10 pA). The most likely cause in our situation is fixturing differences. While both measurements were made using the same fixture, there were some differences in how the measurements were made. The Keithly picoammeter was plugged directly into the current path leading from each of the operational amplifier terminals with heavily shielded probes. This eliminated all circuit components except for the small stretch of wire between the probe terminals and the OP 15A. The current path for the integrated capacitor test however includes switches S3 and S4. It's possible that these switches had some effect on device leakage current. In addition the wiring on the test fixture was less shielded than that of the Picoammeter probes giving another possible source of error. These factors could easily account for a 10 pA difference in current readings.

It should be pointed out however, that use of the ICap method still is much more accurate than the standard method to measure leakage current for this particular case. Under normal conditions the A312 could not make precise measurements of this parameter, use of the ICap method gives this tester the capability of making a much more accurate measurement.

Conclusions: Based on these findings, we determined that the Integrated Capacitor method can make precise measurements of very low leakage currents. The method is also easy to implement, requiring simple components and a controller to insure that the voltage measurements are made at accurate time intervals. The ICap method has considerable potential since a large number of operational amplifiers can not be tested effectively using the old series-4000 test method for leakage currents. We feel that for low leakage current operational amplifiers (such as the sample OP 15A), this method is superior and should be used. While use of a picoammeter (such as the Keithly 485) may produce

more accurate results, the ICap method provides an acceptable alternative if such a meter is unavailable. This method was included in the operational amplifier series-4000 test method as an optional measurement technique for leakage currents. It is also referenced in the comparator test method.

5.1.4.2 Digital Signal Processing Techniques

The Digital Signal Processing (DSP) test methods developed for this contract are centered around the testing of flash data converters. These devices are high-speed A/D converters made up of high-speed comparators connected in parallel. Each comparator provides a threshold measurement for its particular transition level. Each converter is made up of about 2^N individual comparators so that an 8-bit converter can be made up of from 255 to 257 comparators. As converters these devices can be tested using static test methods, but to fully evaluate these parts they should be operated at frequencies close to those used in actual applications.

Test Device: To gain experience and insight into DSP test methods, a relatively low speed analog-to-digital converter (AD7580) was selected due to the availability of dynamic performance data from the manufacturer. The AD7580's principal specifications are as follows:

Full Scale Analog Input	up to 20 KHz
Resolution	10 bits
Integral Nonlinearity	$\pm$ 1 LSB
Differential Linearity Error	$\pm$ 0.9 LSB
Conversion time	16.9 us (minimum)
Sampling rate	50 KHz
Signal-to-Noise-Ratio	55 dB min
Total Harmonic Distortion	-58 dB max
Span	2 V_{REF}
V_{REF}	2.5 V
Clock Range	250KHZ - 20MHZ

Hardware: The test hardware for the evaluation consisted of an Advantest T3381 VLSI digital test system and an HP3335B precision synthesizer used to supply the analog input. We were able to use a digital ATE for this evaluation because of the Data Failure Memory (DFM) option of the T3381 which allows the capture of output codes of the ADC. The DFM is used in conjunction with a test pattern to record each vectors' status, and has a memory capacity of 2K words. A functional test pattern was subsequently developed and contained 2048 vectors. Each vector provided all the appropriate timing signals required to initiate the start of a conversion cycle and established the time when to sample the 10 digital outputs after completion of the conversion. The contents of the DFM is then read and stored in a separate data file for later DSP processing. By repeatedly running the test pattern and reading the contents of the DFM, the large number of samples required for the histogram test can be obtained.

Software: Data analysis was performed on a VAXstation II using VAXlab, a laboratory signal-processing and graphics package software routine obtained under license from Digital Equipment Corporation. These call routines formed the basis of an interactive menu driven program written in "C" which allowed an operator to customize individual plots. Included in the signal-processing section were routines to calculate Fourier transforms, determine correlation functions, apply digital filtering, apply any of five spectral windows, compute power spectrum, phase relationship and spectral amplitude, and perform interval histogramming.

Method Description: Using this test setup, the following computations and analysis can be made:

a. Sinusoidal histogram plot of output codes illustrating missing codes.
b. Differential linearity.
c. Integral linearity.
d. Spectral response and signal-to-noise ratio.
e. Harmonic distortion
f. Normalized transfer function (input voltage vs output code).

The sinewave based histogram is particularly useful as a basis for all tests, as this waveform can be readily implemented with extreme accuracy. Care must be taken to ensure that waveform sampling is random otherwise histograms will contain missing codes. This is accomplished by ensuring that the ratio of output samples taken to the number of sine wave waveforms sampled is a prime number. The actual counts of each output code can then be used as the basis for the derivation of differential linearity error, integral linearity error, and transfer function. In using the sine wave generated histogram to derive these parameters, a probability weighting function must be used as some codes are more likely than others.

The probability of a code occuring for a sinusoidal input waveform is given by the expression:

$$P(i) = \frac{1}{\pi} \sin^{-1}\left[\frac{V(i - 2^{N-1})}{A2^N}\right] - \sin^{-1}\left[\frac{V[(i-1) - 2^{N-1}]}{A2^N}\right]$$

where V = full scale range of the ADC
N = number of bits in the ADC
i = code
A = peak amplitude of the input sinewave

After obtaining the number of counts for each code, the dynamic differential linearity error in least significant bits (LSB) can be computed.

$$DLE(i) = \frac{\left[\frac{n(i)}{N_t}\right]}{P(i)} - 1 \text{ in LSB}$$

where $n(i)$ = number of counts of code i
N_t = total number of counts

Plots of DLE versus code can then be made and examined for missing codes. Integral linearity error for an end point to end point fit can be computed from differential linearity error by computing an array of ILE(i) values from DLE(i) values. The equation defining this relationship is:

$$ILE(i) = ILE(i-1) + \frac{DLE(i) + DLE(i-1)}{2}$$

Integral linearity can be plotted as a function of code so as to determine whether extreme values exceed specification limits.

Signal-to-noise ratio (SNR) can be computed by applying the fast Fourier transform to the collected data and plotting the resulting spectrum. The computed spectrum is then "notched out" by setting the frequency bins associated with the fundamental to zero. The RMS of the rest of the spectrum is designated as noise. Signal-to-noise ratio is then determined by computing the ratio of signal to noise.

Harmonic distortion can be computed from the ratio of the sum of the squares of the RMS voltage of the harmonics to the RMS voltage of the fundamental. For the device under study, the total harmonic distortion (THD) is:

$$THD = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6 are the amplitudes of the individual harmonics.

Verification: The DSP techniques were verified under the following test conditions:

Temperature	= +25°C
Clock rate	= 2.5 MHz
VDD	= +5V
ADC test sample rate	= 51.2 KHz
Input test frequency (FFT)	= 3.491 KHz

Maximum input test frequency = 20 KHz
Number of FFT samples = 2048
Input sinewave amplitude = 4.982 Vpp
Number of histogram samples = 200000

To obtain a histogram plot, a sinewave input was applied at a frequency of 3.49121 KHz and the devices output vectors were sampled at 50000 samples per second. 204701 samples were collected for each run. This ensured that a prime number of sine waves (143) were sampled for 2048 output data samples. This procedure was completed 100 times to provide a total of 204800 data samples for histogram and FFT generation.

Figure 5.1.4.2-1 displays a histogram plot for an AD7580. There are no missing codes and the histogram appears to be equivalent to that displayed in the manufacturer's literature. The differential linearity error (DLE) computed from the histogram is $\pm$ 0.65 LSB which is within specification. Figure 5.1.4.2-2 is a plot of differential linearity versus output code. The integral linearity error computed from the histogram ranges from +0.5 LSB to -1.0 LSB. This result was obtained by integrating the differential linearity error as explained previously and is shown in figure 5.1.4.2-3. Finally, figure 5.1.4.2-4 displays the spectral response of the AD7580. From this plot SNR and THD can be obtained. THD is -64.30 db and SNR is -42.9 db which is out of specification. Possibly a higher quality signal generator is required.

Conclusion: Because of the high conversion rates for flash A/D converters, DSP techniques are needed to make dynamic measurements of several critical parameters. Based on our evaluations, we included the DSP techniques described in this section as the specified method for measuring flash converter parameters.

5.2 Test Method Selection Criteria

Following the test method identification study of section 5.1 above, we made a selection of tests to be included in the new series-4000 test methods. The criteria adopted for selecting amongst the various test approaches identified for each parameter were that the method be:

1. Consistent with the definition of the parameter and the normal application of the device.

2. Adaptable to both bench and ATE test approaches.

3. Specified in one or more MIL-M-38510 slash sheets for linear devices.

4. Established in industry.

5. Offering significant improvments in resolution, accuracy or speed.

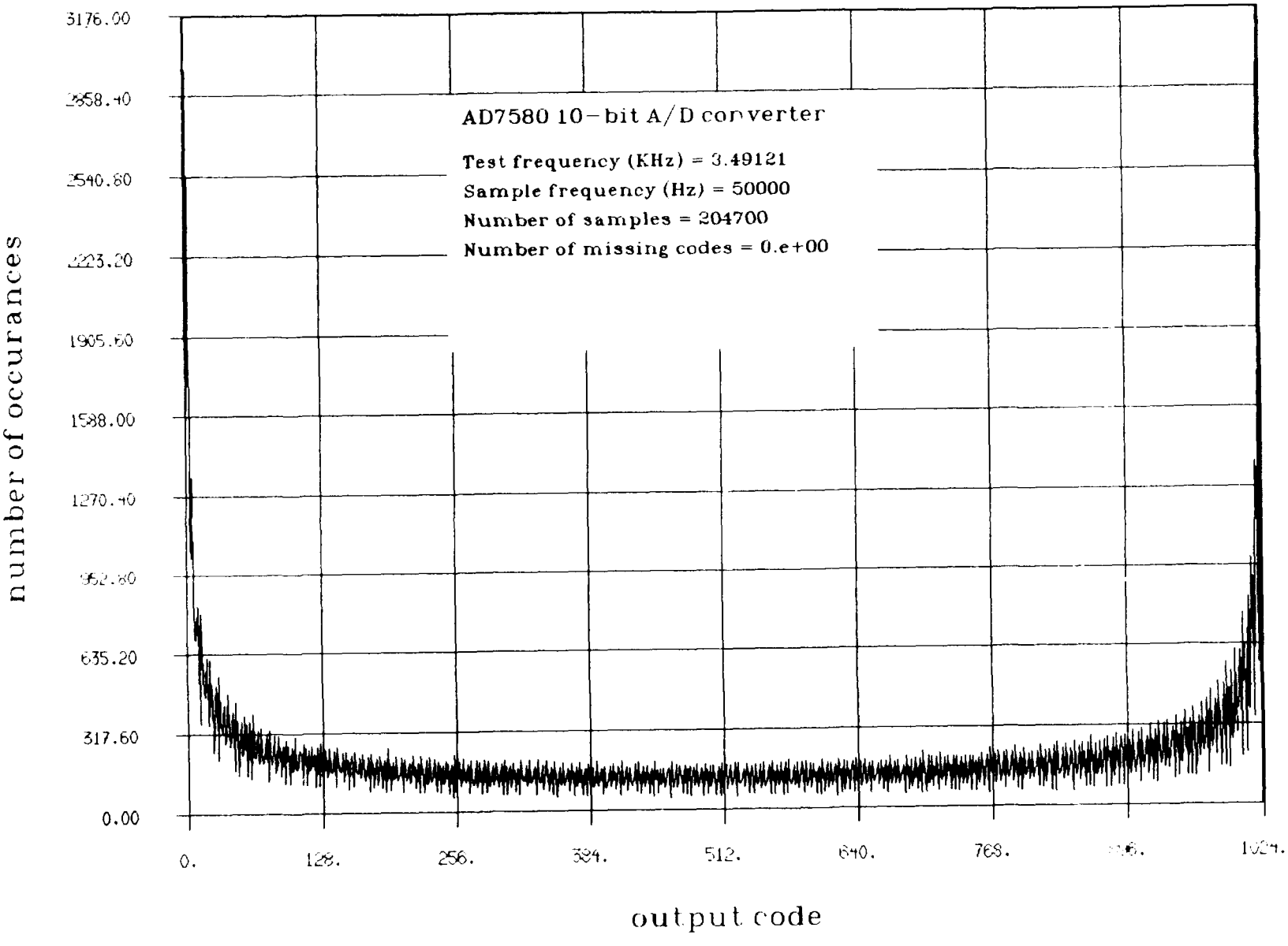


Figure 5.1.4.2 - 1. Distribution of Output Codes

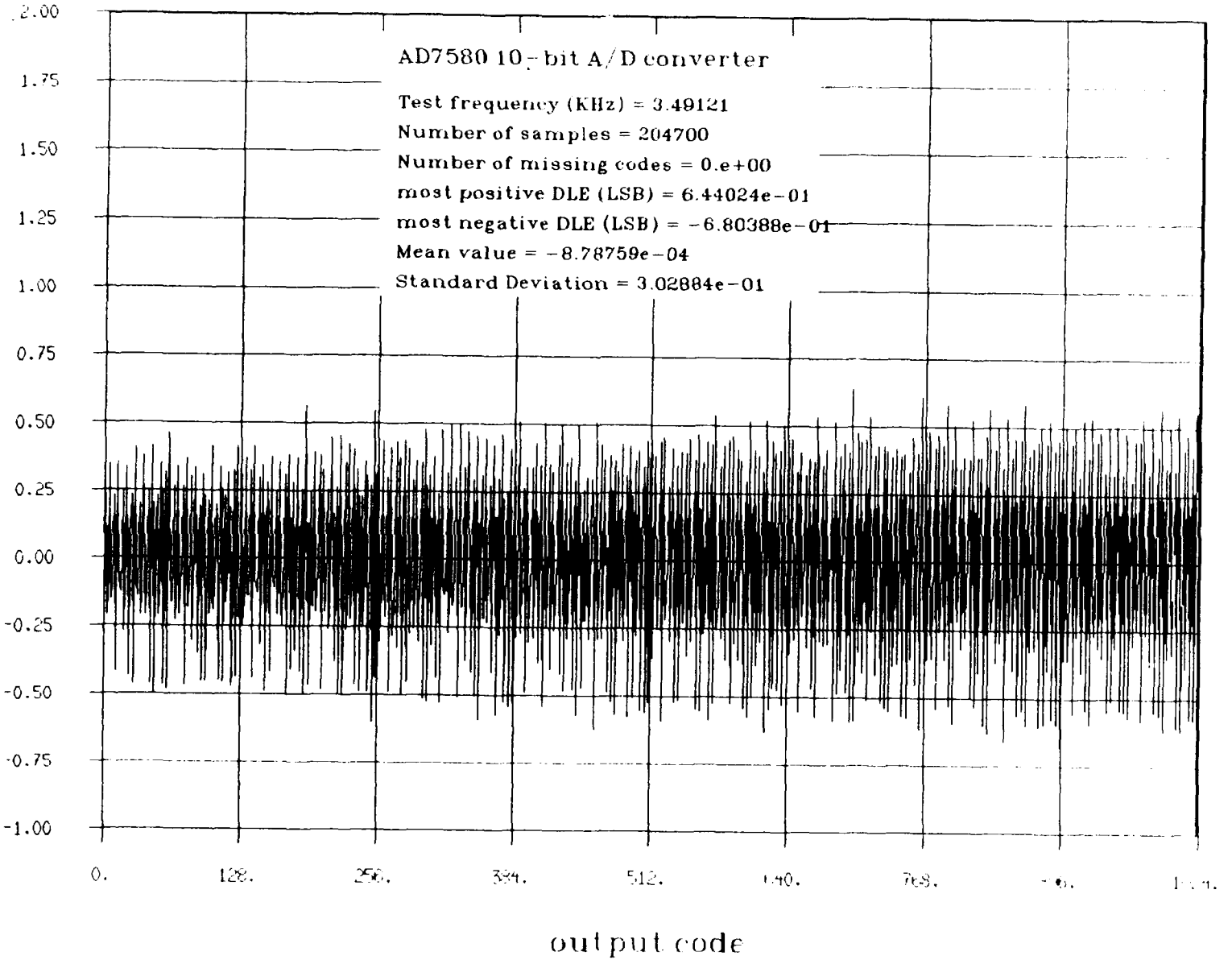


Figure 5.1.1.2 -2 Dynamic Differential Linearity

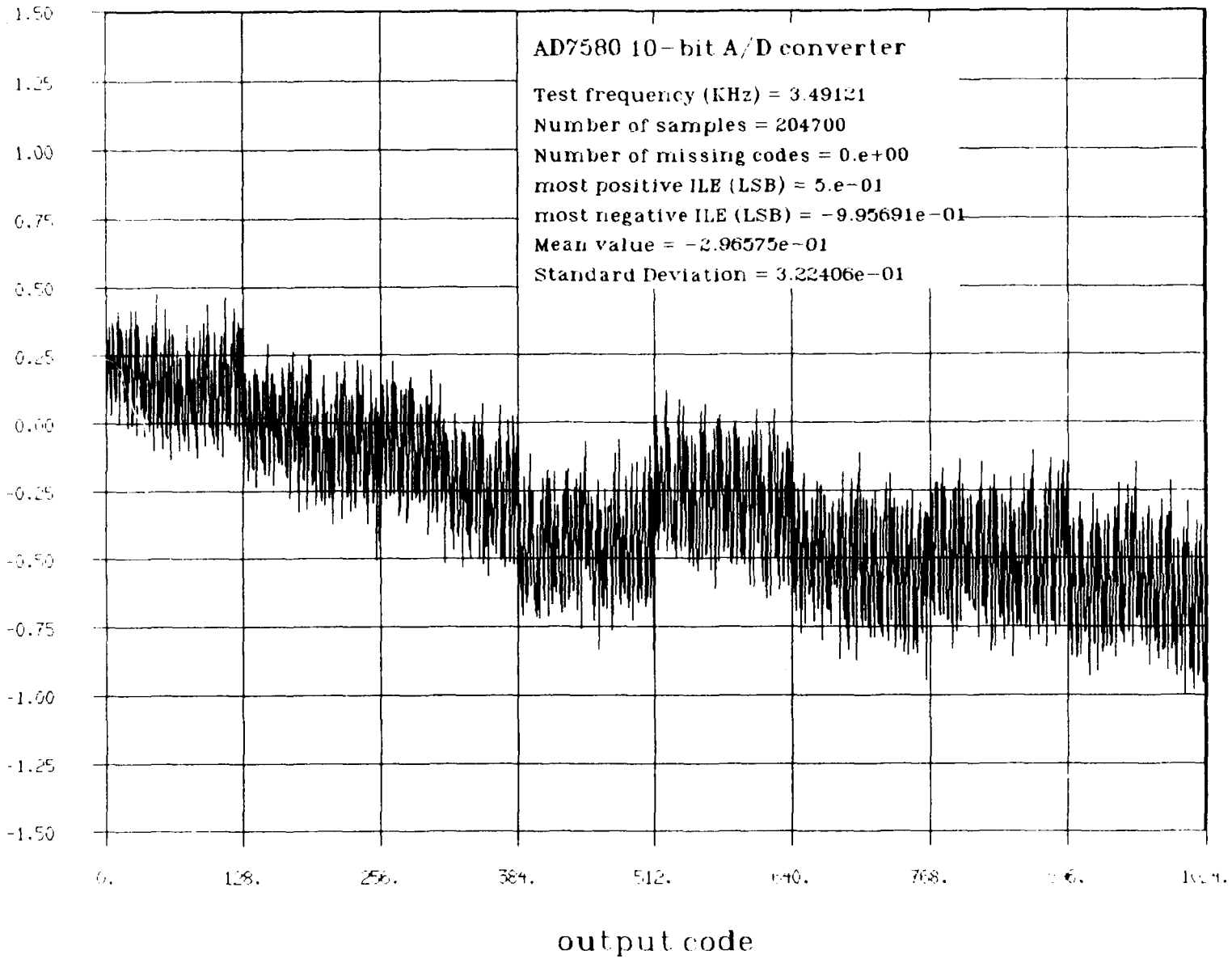


Figure 5.1.4.2-3. Dynamic Integral Nonlinearity

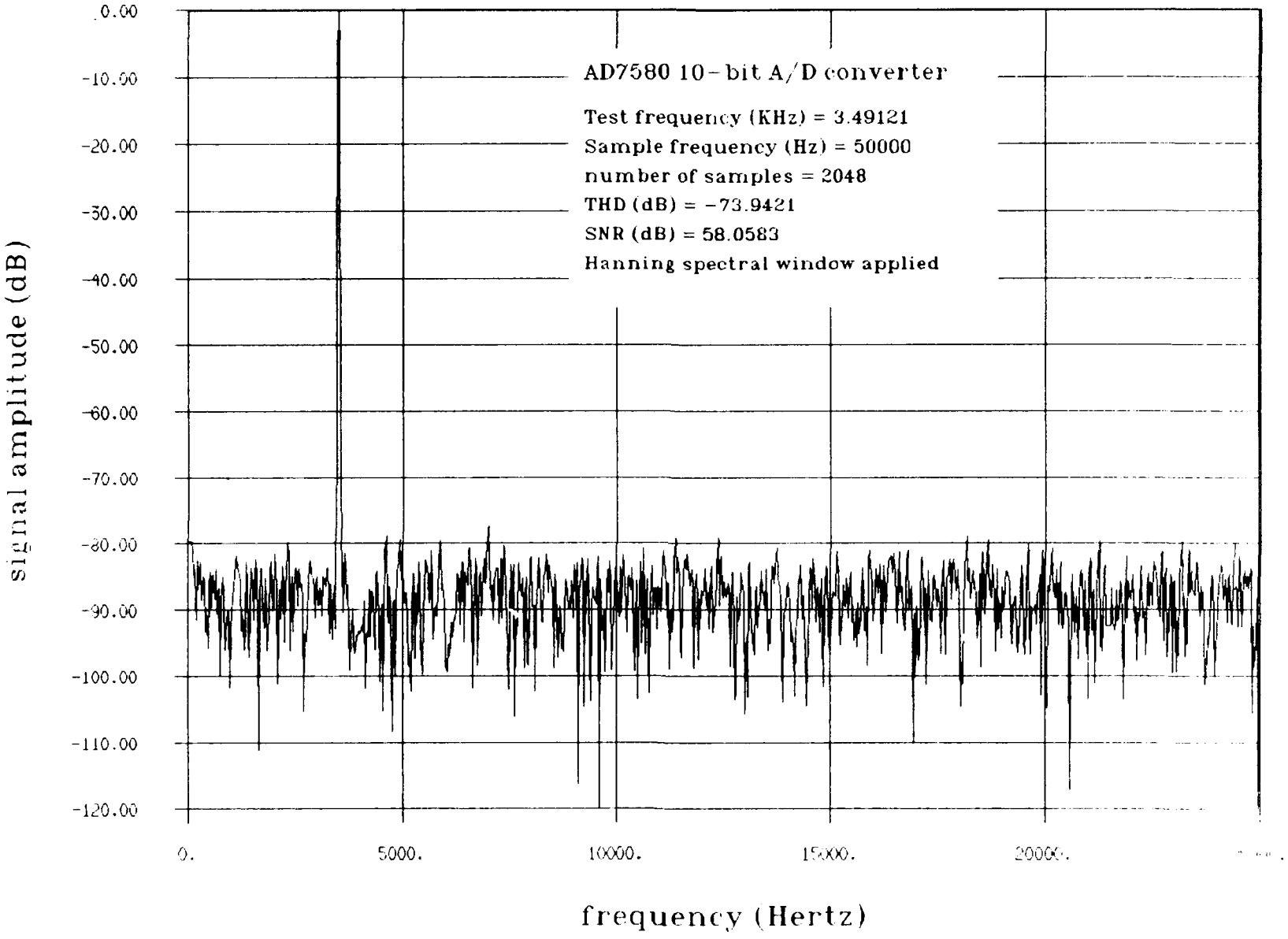


Figure 5.1.4.2-4 Dynamic Spectral Response

Conformance of selected test methods to the first two criteria was considered essential while preference was given to methods meeting the remaining three criteria. Where application of the criteria led to alternative methods, we put the choice to Occam's Razor: other things being equal the simplest approach was chosen. In section 7 we refer to these criteria in discussing the test approaches selected for the generic families.

A surprising result of application of the criteria was that few of the existing series-4000 test methods proved suitable for incorporation into the generic specifications. As noted in section 5.1.1, the older methods are oriented towards testing of operational amplifiers as small signal ac linear amplifying devices. However, the parameter definitions adopted for this program, as well as the existing slash sheets for operational amplifiers call for static and large signal dynamic tests. Moreover, the static tests of the 4000 methods show a test circuit employing direct feedback. The preferred approach in the slash sheets and in industry practice is to use a nulling amplifier loop.

5.3 Test Circuit Development

Test circuit development proved to be one of the most difficult tasks in the development of generic test methods. The difficulties arose out of conflicting objectives and were resolved by determining the most essential requirement. Unlike digital test configurations which involve sets of identical inputs and outputs, each having two states, linear circuits test configurations have many varieties of both input and output and frequently incorporate feedback circuitry between input and output. As a result, linear test circuit design involves complexities beyond the connection of input drivers and output comparators to the test device. This section describes the main tradeoffs that were made in test circuit development to accommodate the special problems of specifying generic linear device test circuits.

Our initial desire to have each test circuit sufficiently detailed to enable easy duplication proved unrealistic because of the wide variation of parts within a family. We decided in favor of clearly showing the principle of the measurement and identifying the signal, control, and measurement terminals on the device in test. Another initial objective which proved unrealistic was to include in the new test methods details of test system loading, power supply decoupling and any stabilization circuitry required for additional linear components included in the test circuit. These aspects of the test circuit are dependent on the specific test instrumentation, test fixture construction and wiring, and on the specific performance of individual members of the device family. As a result, these details did not fit within the concept of a generic test method. However, we indicated in the drawings or footnotes wherever it

was clear that special measures should be taken on the basis of the generic family characteristics or the basic test circuit design. In conclusion, the test methods assume that the test engineer or technician is familiar with linear equipment and fixturing. Moreover, where device connection and stabilization requirements differ within a family, these requirements should be specified in the procurement document for that device.

It was also considered desireable to minimize the actual number of test circuits by combining measurements in a single circuit. In particular, it was a goal to make all static parameter measurements in a single circuit. This avoided creating many, essentially similar, circuit diagrams. At the same time we did not want the circuits to become so overly complex through the inclusion of many switches, relays and auxiliary components that the principle of each measurement became obscured. A good example of a circuit combining static tests is the nulling amplifier loop circuit provided for the operational amplifier. Inclusion of a modest number of switches enables measurement of all static parameters in a single circuit. The accompanying test table in the new series-4000 document shows the switch configurations for each measurement.

Another tactic adopted for the sake of clarity in defining the test method was to include more stimulus sources and meters than would be needed in a practical test setup. In some circuits, for example the static test circuit for analog switches, the measurement principle was best illustrated by including multiple sources and meters rather than creating a complex circuit with many reconfigruation switches. In a practical bench circuit or in ATE, the sources and meters would be reconnected manually or automatically to perform different tests. Moreover, proper test procedure would deduct any superfluous instrumentation loading the test device.

In conclusion, the development of generic test circuits called for compromises which were decided in favor of clearly defining the principle of measurement, minimizing the number of test circuits and limiting the complexity of the circuits.

5.4 Specification of Test Equipment

The specification of test equipment to be used in generic test methods poses special problems. The specification must be generic enough to accommodate testing of a family of devices with widely different performance levels requiring different measurement accuracies. It also must be applicable to the various approaches to test implementation: bench test, bussed assemblies of instruments, and full automatic test systems. The specification of test equipment for generic test methods thus has two aspects, functional specification and accuracy specification.

5.4.1 Functional Specification

The approach adopted in defining test equipment was to specify the test instrumentation as functional modules. Each piece of equipment needed to stimulate, measure, or control the device during the test is given a simple functional description. The minimum requirements of the equipment are stated in terms of functionality, accuracy, and resolution. These descriptions should enable the test engineer to select equipment for bench or bussed system tests from amongst the great variety of instruments available, and should also enable the engineer to determine whether a particular ATE system is capable of the measurement. This approach concides with that in the older series-4000 methods. The MIL-M-38510 slash sheet specifications for the most part follow this method of specifying test equipment, however, in some cases a specific instrument is called out with the phrase, "or equivalent" added. Where we have adapted test methods from the slash sheets, we have replaced citations of specific model instruments with a functional description of the instrument requirements, however, in one or two cases, where it appeared helpful, we have cited a specific instrument model as examples of the type of equipment to be used.

The functional module names carried over from the old 4000 specifications include oscilloscope, pulse generator, signal generator, ac voltmeter, dc voltmeter, dc current meter, distortion meter, and noise generator. The elemental nature of these test equipment modules has enabled the test methods to retain their validity as test equipment has evolved since the 1960's and they should continue to serve as equipment grows even more sophisticated. However, we did find it necessary to update this list with the addition of one functional module. We have introduced the functional description "programmable voltage source" to serve the requirement of voltage generation in test circuits that employ automatic adjustment of an input voltage. This functional module provides an analog voltage of specified resolution and accuracy when programmed with a digital input. In actual hardware, this function is realized by many modern bench type voltage sources which are either keyboard programmable or receive digital programming instructions from a bus connected controller. Moreover, all linear ATE system voltage sources fit this description. We have used this functional module in several test methods, in particular it has been used to implement the various digital-to-analog converter circuits that have been described in the slash sheets test circuits for ADCs and DACs.

5.4.2 Accuracy Specification

Under this heading we studied the entire range of specifications for test instrumentation that may be critical to a specific test for a specific device. These specifications include accuracy and resolution of voltage, current, and waveform stimulus and measurement equipment. Also, harmonic distortion, bandwidth, response time, input/output impedance and dynamic range are other

factors that can effect a particular measurement. The measurement technique employed by an instrument may also be a factor in some tests as with an analog versus a digital oscilloscope.

Obviously, these requirements will vary greatly in testing different performance levels of devices in a family. The precisions of measurement demanded by an 8-bit and a 16-bit digital-to-analog converter are many orders of magnitude apart. Specifying equipment beyond the requirements for a given device would impact the cost of military systems. The sensitivity of the test community to the economic impact of accuracy requirements was evident during the industry review of draft specifications. It was noted immediately that the proposed specification for 0.1% accuracy in supply voltage measurements was beyond that required in slash sheet specifications. The requirement was therefore modified to 1.0%.

It was clear that the accuracy specification of the test instrumentation would need to be relative to the tolerance specification given in the procurement document of the device in test. This requirement also applied to the existing series-4000 test methods and is handled in some cases by specifying accuracy as a percent of parameter tolerance and in other cases by the broad requirement that the instrument not degrade the measurement. Faced with the same problem in preparing the generic test methods, we endeavoured to use a numerical specification relative to device parameter tolerance for each functional equipment module. Generally, these accuracy specifications are expressed as a percentage or fraction of a least significant bit.

In cases where it appeared that the measurement technique might impact accuracy as in digital sampling rates for flash converter measurements, the requirement has been specified so as to avoid this problem.

In summary, the generic test methods have specified test equipment accuracy so as to assure that measurements made correctly test each device to its specified levels. However, the responsibility remains with the test engineer to correctly interpret the test equipment requirements in terms of the procurement document specifications for the device.

6.0 TEST METHOD PREPARATION

The final stage of the program was the preparation of the new series-4000 drafts outlining the generic methods. A format similar to that used in the existing series-4000 methods was chosen and the new drafts developed along these lines. Once initial drafts of the new test methods were completed, they were submitted to RADC for review. This process consisted of reviews by RADC and several industry members of the JEDEC JC-41 committee. This section of the report describes in detail the format used for each of the test methods, and the review process used on the completed drafts.

6.1 Format Description

The basic format for each new test method remained similar to that used in the existing series-3000 and 4000 methods. Each test method is divided into six distinct sections which are described as follows:

Purpose: Section 1.0 of each method is the Purpose section which lists what types of microcircuits the document applies to, and the parameters that are covered in the test specification. More importantly, it includes definitions of all important terms used throughout the method. This includes descriptions of each parameter and in some cases equations needed to derive them.

Apparatus: Section 2.0 is the Apparatus section which describes the test equipment needed to perform all of the necessary measurements. For all test circuits used in the test method, each major piece of equipment is identified and its capabilities listed. As mentioned in section 5 of this report, equipment is specified by function and minimum capabilities without reference to any particular part number or manufacturer. The only exception to this is in the Operational Amplifier test method where the Noise Density test circuit requires the use of rather specialized equipment. Passive components that are integral to circuit operation (such as load resistors or gain setting resistor networks) are also specified in the apparatus section. Note that depending on the device type being tested, not all of the equipment in this section may be required to perform a complete test.

Procedure: Section 3.0 is the Procedure section which outlines how each measurement is made. Typically, the first paragraph in this section discusses the general technique or approach used to make these measurements. Each figure used in the test method is also identified as well as the parameter(s) it is applicable to. Any special nomenclature used in the discussion of the test procedures is also described here. The remainder of the Procedure section describes in detail how to perform each individual measurement. Typically the tests are grouped such that static parameter test procedures are discussed first, followed by dynamic procedures. Reference is made to necessary

figures and equations are fully derived for each parameter (in some cases this derivation may be part of the definitions in section 1.0, or part of the test table). As previously discussed in section 4 of this report, several parameters can be measured using the existing series-3000 digital test techniques. These parameters are also listed in the Procedure section with the appropriate series-3000 method being called out as the recommended measurement technique. For the Operational Amplifier and Voltage Comparator test methods, alternate test procedures are described to give increased flexibility in making some measurements. These are included at the end of the Procedure section.

Summary: Section 4.0 is the summary section which lists all information that must be obtained from the device procurement document to perform complete testing.

Test Table: Following the text of each test method is the test table. This is included in all of the test specifications except for Flash Converters. The test table summarizes the conditions (i.e., status of switches, power supplies and current supplies in the test circuit), measurements, and equations needed to obtain a value for each parameter included on the table. Note that in most cases the test table only covers the static parameters for a given linear family. This is because most dynamic parameters require test circuitry much different from the static parameters, and thus do not fit within the context of the test table columns and conditions. To compensate for this, information of this type is included in the form of tables or notes on the dynamic test circuit diagrams.

Test Figures: The final portion of each test method consists of the test figures and diagrams. This includes all test circuits, waveform diagrams, and explanatory figures referenced by the test method. The composition of the test circuit diagrams has been previously discussed in section 5.3 of this report.

By using this format we were able to develop complete and concise test procedures to measure selected parameters of each linear device family covered by the program. These procedures could be used by a test engineer to evaluate a variety of linear devices in a consistent manner. An overview of each test method developed for the contract is included in section 7 of this report.

6.2 Industry Review

The final objective of this effort was to recommend a standardized test methodology for linear devices. To be effective, the proposed test methods should be readily understood and implemented by suppliers of linear devices to military programs. To assure that the objective was met, RADC circulated preliminary drafts of all the proposed series-4000 generic test methods among domestic suppliers of linear military specification parts.

methods among domestic suppliers of linear military specification parts.

The review process began in the spring of 1990 after the initial drafts of the test methods had been reviewed by RADC and revised by Boeing. Copies were delivered to each company representative on the JEDEC JC-41 committee in May. This committee was an appropriate sounding board for the new methods since all suppliers of MIL-SPEC linear parts are represented. Several companies responded, submitting comments that ranged from the simple clarification of terms and definitions used in the test methods to detailed examinations of specific test techniques.

All industry inputs were initially reviewed by RADC. Suggested changes were evaluated then collated and forwarded to Boeing for incorporation into the final drafts of the proposed test methods. The comments received from industry were very insightful and definitely improved the overall quality of the test methods.

6.3 Summary

The end result of this phase was the completion of proposed series-4000 generic linear test methods designed to cover 11 families of linear device types widely used in military systems. The proposed test techniques were designed for the most part to reflect current industry practice with a few selected new methods being introduced. Drafts were developed using a format similar to that of existing series-3000 and 4000 test methods. A review by members of the JC-41 committee resulted in some revisions and final drafts were submitted to RADC in August 1990. The next section of the report, section 7, gives an overview of each of the test methods, including a description of the the test approach and the rationale for selection of the various test procedures. Unofficial copies of the new 4000 Series Linear Test Methods have been included in appendix A of this report.

7.0 OVERVIEW OF TEST METHOD SPECIFICATIONS

This section consists of individual overviews of the 11 new series-4000 test methods prepared in this program. In these overviews the generic range of devices intended to be covered by each method is described and, in addition, the existing MIL-M-38510 slash sheet parts specifically covered are listed. The actual parameters that were included in the generic test method are listed for each family. Finally, for each test method, the test approach or approaches are summarized briefly.

7.1 Analog Multiplier

Range of Devices Covered: The test procedure is applicable to integrated circuit hybrid circuit analog multipliers operating in one to four quadrants having x and y or x,y and z inputs.

The following slash sheet was reviewed in detail during preparation of the generic test method specification:

/139 - Linear, internally trimmed hybrid and monolithic analog multipliers; Commercial types 534T, 534S, 532S and 4213.

This is the sole slash sheet for analog multipliers. We also reviewed parameter definitions and specifications in the Burr-Brown and Analog Devices databooks.

Selection of Parameters: Parameter selection was based upon the slash sheet test requirements. Sixteen parameters are covered by this generic test specification as follows:

Multiplier Accuracy
Output Voltage Offset
Feedthrough Error
Nonlinearity
Small Signal Amplitude Error
Input Offset Voltage
Input Bias Currents
Input Offset Currents
Power Supply Rejection Ratio
Common Mode Rejection Ratio
Output Voltage Swing
Power Supply Current
Output Short Circuit Current
Settling Time
Slew Rate
Wideband Noise

Test Approach: Analog multipliers have many parameters in common with operational amplifiers, however, the actual input currents and offset voltages of the devices examined are an order of magnitude larger than those of typical operational amplifiers. Therefore, the approach adopted for testing of static parameters

measures current and voltage directly at the inputs and outputs of the device. This is in contrast to the more sensitive nulling amplifier approach used for operational amplifiers.

A single test circuit is defined for the static parameters plus small signal gain, settling time and slew rate. One additional circuit defines the noise test setup.

7.2 Analog Switch

Range of Devices Covered: The slash sheets and commercial specifications reviewed for this generic test method confirm that it is applicable to single and multiple channel JFET and CMOS switches. Similarity of design indicates that the procedures will also be applicable to CMOS multiplexers and crosspoint switches.

The following slash sheets were reviewed in detail in preparation of the generic test method specification:

/58C - CMOS positive logic analog switches; commercial types 4016A, 4066A, 4016B, 4066B.

/111 - analog switch with driver (J-FET); commercial types DG181A, DG182A, DG184A, DG185A, DG187A, DG188A, DG190A, DG191A.

/116 - CMOS analog switch with drivers; commercial type DG300, DG307.

/123A - CMOS negative logic analog switches; commercial types DG 200, 201.

Also reviewed were Siliconix Analog Switch Databook, National CMOS Logic Databook, Harris Linear & Data Aquisition Products Databook (1977) and Taub and Schilling.

Selection of Parameters: The selection and definition of generic parameters for analog switches presented unique problems due to different physical implementations of the switch channel. The analog switch devices specified in existing slash sheets include single n-channel JFET switches and CMOS paralleled n-channel and p-channel MOSFET switches. The latter which may be fabricated in junction isolated or dielectrically isolated technologies. Parameters and tests for JFET switches given in the slash sheets always distinguish the source and drain terminals. For CMOS switches this may or may not be done. The interpretation of the generic test specification for CMOS parts should follow the slash sheet or procurement document. If source and drain terminals of a CMOS switch channel are designated then the test procedures should follow this distinction otherwise "IN" and "OUT" channels may be arbitrarily biased. The static test circuit in the test procedure is applicable in either case.

The strategy adopted to achieve generic parameter tests was to use the descriptors "input" and "output" in the parameter names. The relation between source and drain and input and output for different switch types is delineated in the definition or procedure. Eighteen generic test procedures were specified as follows:

Channel Resistance
Control Input Current
OFF Input Current
OFF Output Current
ON Output Current
Channel Leakage Current
ON Output Voltage
Power Supply Current
Charge Transfer Error
Crosstalk Voltage
OFF Isolation
Switch On Time
Switch Off Time
Switch Propagation Delay
Break-before-make Time
Control Terminal Capacitance
Switch Input Capacitance
Switch Output Capacitance

Note that in some cases parameters may only be applicable to one type of analog switch (either FET or CMOS). This distinction is made in the procedure section of the test method.

Test Approach: One universal test circuit has been specified which is illustrative of the configurations required for all static tests for analog switches. An accompanying table indicates the terminal at which current or voltage is forced, that at which the measurement is made, and the required control inputs. Separate test configurations and waveform diagrams are included for dynamic tests.

7.3 Analog-to-Digital Converters

Range of Devices Covered: An early decision was made to limit the scope of this generic test method to successive approximation type analog-to-digital converters. Of the two other approaches to integrated ADCs, the multi-comparator type is covered by the flash converter generic test method, while the integrating type AD converter is more limited in application and in performance over the military range (reference 8). Those types for which current slash sheets exist are all successive approximation types.

The following slash sheets were reviewed in detail in preparation of the generic test method specification:

/120 - hybrid 12-bit successive approximation analog-to-digital converters; commercial types 5200, 5201, 5202, 5203, 5204, 5205, 5206, 5207, 5210, 5211, 5212, 5213, 5214, 5215, 5216, 5217.

/134 - monolithic 10-bit successive approximation A/D converters with 3-state buffered outputs; commercial type ADC571.

/140 - monolithic and hybrid microprocessor compatible successive approximation type 12-bit analog-to-digital converters with buffered outputs; commercial types 574, 564.

Selection of Parameters: The parameter selection for the ADC generic test method covers all those parameters needed to assure the performance of a successive approximation type ADC. Our initial matrix evaluation brought out a number of additional parameters related to abbreviated code test schemes for determining the worst case linearity of the part tested, for example, the Major Carry Error parameter. Where such schemes are to be used, they should be specified in the procurement document. This generic test procedure describes the method for making the basic transition point measurement on which all linearity parameters are based. The definition for linearity adopted is the "end point" linearity. This definition provides the best basis for comparing performance of different ADCs. The "best fit" linearity used adopted by some manufacturers can not be worse than the end point linearity.

The only generic time related parameter that we identified for successive approximation ADCs was the maximum conversion time. This parameter however is determined by the clock rate of the device. Thus conversion time by definition will always be valid so long as the device is functional and therefore is not normally tested in practice. However, we have included a definition of this parameter in the test method.

Seventeen test procedures were included in the final version of the ADC test method as follows:

Zero Voltage Error
Bipolar Zero Voltage Error
Positive Full Scale Voltage Error
Negative Full Scale Voltage Error
Code Width Error
Unipolar Offset Error
Gain Error
Integral Linearity Error
Differential Linearity Error
Transition Uncertainty
Power Supply Sensitivity Ratio
Power Supply Current
Input Leakage Current

Output Voltage Levels
Output High Impedance Current
Output Short Circuit Current

Test Approach: The basic measurement for determining the bulk of ADC parameters is the code transition point. The approach to this measurement adopted in the test method is known as the digital loop method. The procedure involves a feedback adjustment of the analog input to the device in test until the desired code transition occurs. The essential hardware elements include a digital comparator to determine the relationship between the ADC output and the selected code, controller circuitry to adjust the input, and a digitally programmable voltage source that provides the analog signal. Some form of this arrangement is described in each of the slash sheets examined in preparing the procedure. The controlling function may be implemented in logic hardware or accomplished by the insertion of a computer in the loop. A sample search algorithm for finding the transition point selected is diagrammed in the procedure. Any suitable successive approximation search algorithm is allowed. However, it is essential that the transition always be approached from the same direction to eliminate the effect of hysterisis.

7.4 Digital-to-Analog Converter

Range of Devices Covered: This generic test method covers unipolar and bipolar DACs having either current or voltage outputs and either internal or external reference voltage sources. The limit of resolution that can be tested is determined by the accuracy of the reference voltage source used in the test procedure. The procedure calls for an accuracy equal to 1/16 lsb of the device in test.

The following slash sheets were reviewed in detail in preparation of the generic test method specification:

/113 - 8-bit digital-to-analog converter; commercial type DAC-08, DAC-08A.

/121A - 12-bit digital-to-analog converter; commercial type 562, 563, 565, 566.

/127A - 12-bit digital-to-analog converter; commercial type 7541.

/133A - 10-bit digital-to-analog converter; commercial type 561.

/137A - range programmable, voltage output 12-bit digital-to-analog converters; commercial types DAC-87, DAC-97.

/144 - 8-bit digital-to-analog converter with microprocessor interface; commercial type AD558T.

Selection of Parameters: Fourteen DAC parameters were selected for inclusion in this generic test method. Twelve of these are static parameters, the remaining two are settling time and noise figure. For the linearity parameters, end point linearity was adopted. This is more a conservative rating than best fit linearity and is the method used in the slash sheets examined. The fourteen parameters are:

Output Offset Voltage
Offset Drift
Gain Error
Gain Error Drift
Integral Linearity Error
Differential Linearity Error
Full Scale Output Current
Zero Scale Output Current
Power Supply Sensitivity Ratio
Power Supply Current
Input Current
Settling Time
Internal Reference Voltage
Output Noise Voltage

Test Approach: The reference voltage source approach used for static DAC tests adapts well to both bench and automatic testing. In the method, the analog output of the device in test and an ideal voltage generated by the reference source are summed by an error amplifier. The amplified error voltage is converted to device LSBs and used to compute the various linearity, gain and offset parameter values.

The reference source is required to have an accuracy and resolution at least equal to four more significant bits than the device in test. In practical implementations, the reference source will consist of one or more DACs. Where the resolution of the test device is more than 8- or 10-bits, a trimmer DAC can be used along with a primary reference DAC. The trimmer DAC will have its output voltage brought to the summing node through a precision voltage divider which typically attenuates the trimmer voltage by 1000. It should be noted that the resolution of the primary reference voltage source need not be greater than that of the tested device but the accuracy at each setting must be better than 1/16 lsb. However, to obtain the necessary accuracy in this reference DAC it is customary to use a part having resolution two to four bits greater than the device in test.

7.5 Flash Data Converters

Range of Devices Covered: Devices covered are those A/D converters known as flash converters which have separate comparators for each output decision level. These high-speed devices lend themselves to digital signal processing measurement methods specified in this test method.

The following sources of information and part specifications were reviewed in detail during preparation of the generic test method specification.

Hewlett Packard Product Note 5180A-2 "Dynamic Performance Testing of A to D Converters".

Vendor data for Sipex HS1068 8-bit 20 megasamples/sec A/D converter.

VaxLab guide to the signal processing routines Digital Equipment Corp.

Selection of Parameters: Since parameters were already selected for standard A/D converters, the emphasis on selection of parameters for flash converters was placed on those parameters associated with high-speed signal processing. These included:

Dynamic Differential Linearity Error (DLE)
Dynamic Integral Linearity Error (ILE)
Signal-to-Noise Ratio (S/N)
Harmonic Distortion

Test Approach: The test approach selected consists of applying a pure low distortion sinewave signal at the analog input of the ADC and sampling the output at an appropriate sampling rate. Output sample counts are made for each code. Differential linearity, integral linearity, and signal-to-noise ratio are computed from the code counts using signal processing algorithms. A more detailed discussion of the DSP techniques specified is in section 5.1.4.2.

7.6 Operational Amplifiers

Range of Devices Covered: The generic test specification will be applicable to integrated circuit operational amplifiers having the following descriptions: differential input, wideband, dual, quad, single ended, single supply, high input impedance, low noise, precision.

The following slash sheets were reviewed in detail during preparation of the generic test methods specification:

/101G - single and dual internally compensated operational amplifiers; commercial types 741A, 747A, LM101A, LM108A, LH2101A, LH2108A, LM118, 1558.

/110B - quad operational amplifiers; commercial types LM148, LM149, 4741, 4156, 4136, LM124, LM124A.

/114A - Bi-FET operational amplifiers; commercial types LF155, LF156, LF157, LF156A, LF157A, LF158A.

/119 - Bi-FET operational amplifiers; commercial types 061, 062, 064, 071, 772, LF153, LF412, 074,774, LF147.

/135B - single and dual low offset operational amplifiers including broad, band; commercial types OP-07A, OP-07, 714, OP-27A, OP-227A, OP-37A.

We also reviewed parameter definitions in the PMI, National and Analog Devices databooks and in Gayakwad.

Selection of Parameters: Our initial matrix analysis of selected slash sheet specifications yielded a set of parameters consistent with the original definition of an operational amplifier as a device for computing mathematical functions. A more detailed review confirmed that, although these devices are widely applied as linear small signal amplifiers, slash sheet specifications call out dc tests rather than small signal tests for such parameters as common mode rejection, power supply rejection, channel separation, and open loop performance. In none of the slash sheet specifications studied did we find a requirement for a small signal bandwidth test. We concluded that, since small signal performance is strongly influenced by circuit design and external components, small signal performance tests should be application based rather than generic and should be defined in the procurement document if such performance is critical to the application.

Subsequent to review by RADC, broadband noise and input noise current and voltage densities were added to the initial list of generic test parameters selected by the matrix method. Industry inputs led to the additon of popcorn and peak noise parameters.

The final set of parameters for inclusion in the generic specification follows:

Input Offset Voltage
Input Offset Voltage Adjustment Range
Input Offset Voltage Drift
Input Offset Current
Input Offset Current Drift
Input Bias Currents
Voltage Gain
Output Voltage Swing
Common Mode Rejection Ratio
Common Mode Input Voltage
Power Supply Rejection Ratio
Power Supply Current
Output Short Circuit Current
Channel Separation
Input Bias Current
Settling Time
Rise Time
Slew Rate
Broadband Noise

Popcorn Noise
Input Noise Voltage Density
Input Noise Current Density

Test Approach: All static tests have been combined in a test circuit based on the nulling amplifier approach. Some variation of this circuit is used in all the slash sheet specifications we examined. It is also implemented in the Teradyne A312 automatic test system and in the Tektronix 577 curve tracer. This versatile circuit can be used with inverting or non-inverting amplifiers. Its advantages include keeping the DUT inputs close to ground level for minimum noise pickup and amplification of small offset voltages to measurable levels. Common mode and power supply rejection are measured by offsetting the power supply voltages. Gain measurements are made by measuring the amplified input voltage required for a forced output voltage on the DUT, thus large variations in gain can be accommodated. The nulling amplifier circuit is convenient for measuring input currents, however, very high impedance devices may require use of the integrating capacitor method described in section 5.1.4.1. This method is included in this specification as an optional test method.

A form of the nulling amplifier circuit is also employed for measurement of channel separation in multiple device monolithic amplifiers. This test might have been incorporated in the basic static test circuit with the inclusion of additional components and switches but was diagrammed separately in the interest of clarity. Four additional test circuits are defined for dynamic and noise measurements. General test practice is to use separate test setups for these measurements due to sensitivity to capacitive loading and noise pickup.

7.7 Sample-and-Hold Amplifiers

Range of Devices Covered: This generic specification is applicable to all sample-and-hold microcircuits covered by the slash sheets.

The following slash sheets were reviewed in detail during preparation of the generic test method specification:

/125 - linear sample and hold monolithic silicon integrated circuits; commercial types 198, 5537.

/142 - sample and hold microcircuits; commercial types MN376H/Micro Networks, SHM-4860MM/GE/Datel, THA-05203-1/ILC-DDC 4860-83/Teledyne Philbrick, MTC-0300/Analog Devices.

Selection of Parameters: Parameters were selected to fully test both the operating amplifier portion of the sample-and-hold circuit and the sampling portion. The amplifier tests repeat

many of the procedures in the operational amplifier test method but parameters were included to provide an inclusive test for sample-and-hold devices.

The set of parameters for inclusion in the generic specification follows:

Input Offset Voltage
Input Offset Voltage Drift
Input Offset Voltage Adjustment Range
Input Bias Current
Hold Step Voltage
Gain Error
Feedthrough Rejection Ratio
Hold Droop Rate
Power Supply Rejection Ratio
Power Supply Current
Input Leakage Currents
Acquisition Time
Aperture Time
Transient Response
Noise Voltage

Test Approach: The test approach adopted for static tests of sample-and-hold amplifiers employs a circuit having an error amplifier with a gain of 100. The same circuit is used to measure acquisition time and aperature time using an iterative approach involving repeated sample and hold operations. The acquisition time is obtained by reducing the acquisition pulse width in steps until the allowable error is exceeded. To obtain the aperture time, the time from the end of sample pluse to a full scale change in the input voltage is varied in steps until the specified error margin is exceeded. Two additional test circuits are provided for measurement of transient response and noise.

7.8 Voltage Comparators

Range of Devices Covered: This generic test method covers integrated circuit voltage comparators having single-ended and differential inputs, and incorporating single or multiple comparators.

The following slash sheets, and DESC specifications were reviewed in detail during preparation of the generic test method specification:

/103 - single and dual comparators with and without buffers, low and high speed; 710, 711, LM106, LM111, LM2111, LM119, LM119A.

/112 - dual and high speed comparators; LM139, 193 DESC 5962-86857, 5962-87572.

Selection of Parameters: Parameter selection was based upon slash sheet test requirements. The final set of 17 parameters selected for inclusion in the generic specification follows:

Input Bias Current
Input Offset Current
Input Offset Current Drift
Output Leakage Current
Output Low Voltage
Output Short Circuit Current
Input Offset Voltage
Input Offset Voltage Drift
Input Offset Voltage Adjustment Range
Common Mode Rejection Ratio
Common Mode Input Voltage Range
Power Supply Rejection Ratio
Power Supply Current
Voltage Gain
Channel Separation
Strobe Function Test
Response Time

Test Approach: Two alternative test approaches to measurement of static comparator parameters are specified in this generic test method. The preferred method uses a feedback loop and digital successive approximation circuitry to determine the comparators switching threshold. The test circuit for this method contains an output state detector, binary search circuitry and a programmable voltage source. The programmable voltage source supplies the input to the comparator and the search circuitry adjusts this threshold voltage until an output state transition is detected by the state detector, actually another comparator. To eliminate the effect of switching hysteresis, the search routine given in the test method provides for a reset for the comparator after each transition so that the transition is always approached from the same direction.

The foregoing method departs from the methods defined in the slash sheets. These methods treat the comparator as an operational amplifier and perform static tests with the output biased in the linear region. This approach remains applicable to lower gain devices and is included in the generic test method as an alternative test method.

7.9 Voltage Reference

Range of Devices Covered: This generic test method covers all integrated circuit voltage references including fixed and pin programmable devices.

The following slash sheet was reviewed in detail during preparation of the generic test methods specification:

/128 - linear programmable voltage references; commercial types 584S and 584T.

Selection of Parameters: The similarity of devices within this family facilitated the selection of generic parameters. Essentially all parameters commonly specified for these devices were included in the test method. Nine parameters were selected:

Output Voltage
Load Regulation
Line Regulation
Short Circuit Output Current
Quiescent Current
Turn-on Settling Time
Noise Voltage (Low Frequency)
Noise Voltage (High Frequency)
Output Voltage Temperature coefficient

Test Approach: The relative simplicity of the voltage reference family parts made it possible to present a single illustrative test circuit for all static and dynamic tests and also tests for high and low frequency noise. All measurements are made directly at the input or output of the part in test.

7.10 Voltage Regulator

Range of Devices Covered: This generic specification covers all three terminal fixed and adjustable, negative and positive integrated circuit voltage regulators. The tests are applicable to complex regulators such as the commercial type 723 having additional features such as current limit and frequency compensation, however, for these devices, additional test information and test procedures will be needed in the procurement document.

The following slash sheets were reviewed in detail during preparation of the generic test method specification:

/102 - Precision voltage regulator; Commercial type 723.

/107 - Positive voltage regulator; Commercial type LM140H-05, LM140H-12, LM140H-15, LM140-H24, LM140K-05, LM140K-12, LM140K-15, LM140K-24.

/115 - Negative voltage regulators; Commercial types LM120H-05, LM120H-12, LM120H-15, LM120H-24, LM120K-05, LM120K-12, LM120K-15, LM120K-24.

Selection of Parameters: Parameter selection was based upon the slash sheets evaluated. The final set of 11 parameters selected for inclusion in the generic specification follows:

Output Voltage
Load Regulation

Line Regulation
Standby Current Drain
Adjust Pin Current
Short Circuit Output Current
Minimum Load Current
Voltage Start-up
Thermal Voltage
Output Noise
Ripple Rejection Ratio

Test Approach: The test method provides one circuit configuration for the static tests and pulsed tests. Two additional circuits are provided for ripple and noise tests. All measurements are made directly at the inputs or outputs of the regulator in test.

7.11 Voltage-To-Frequency Converter

Range of Devices Covered: This generic test method is intended to cover all integrated circuit voltage-to-frequency converters.

The following slash sheet, commercial specifications, and DESC specification were reviewed in detail during preparation of the generic test method specification:

/138 - voltage to frequency converter; commercial types VFC32, VFC320, AD650.

DESC 5962-87607.

Commercial types; RM4153, VFC52M, AD652S.

Selection of Parameters: Parameter selection was based upon slash sheet test requirements. Seven linear parameters were selected:

Gain
Gain Error
Offset Voltage
Linearity Error
Input Bias Currents
Low Level Output Voltage
Power Supply Sensitivity

Test Approach: The test approach is based upon the test circuit used for MIL 38510/138 Types 01, 02 and 03. Some features were added from the DESC 5962-87607 specification. With the exception of the output low level voltage, tests are performed by applying a precision voltage at the voltage input and measuring the frequency or voltage at the output with a frequency counter. The low level output voltage is a pulsed measurement and must be observed with an oscilloscope

8.0 SUMMARY AND CONCLUSIONS

Throughout this program we strived to determine standardized methods which could be used to measure parametric performance for a wide variety of linear device types. The end result of this effort is the development of 11 new series-4000 test methods which outline in generic terms the recommended test procedures to be used on several families of linear devices. The existence of such methods will greatly facilitate the testing of linear devices by providing the numerous companies that test such devices with a guideline to how such testing should be performed. Use of these standard methods will allow consistent testing of linear devices and easier comparisons of test data between test laboratories.

As mentioned in this report, our basic philosophy was to develop test methods that could be applied by any competent test facility. To this end, the selected test procedures were kept in the broadest and simpliest terms possible. Our decisions to not specify particular pieces of test equipment and to not include the so called "device specific" parameters were in line with such a philosophy. During the test method selection phase, we tried to include test procedures which had already been accepted by industry rather than developing new techniques. In this regard we were generally successful. The only areas requiring new techniques were in measuring the dynamic characteristics of flash data converters, and input currents on low leakage operational amplifiers. For these areas new procedures were developed and verified to replace the inadequate or obsolete methods.

It should be pointed out to the reader that by adopting the philosophy of developing generic series-4000 test methods, there are some areas that are not completely covered. This is most evident in the area of parameter coverage. While the test methods are geared to provide adequate coverage for M38510 military parts, there are undoubtably some device types which will have parameters not covered by the new series-4000 methods. Thus users of the test methods may be required to develop additional test procedures on their own. However, for the most part these test methods will adequately test the majority of the linear device types available today.

The updating of the existing series-4000 linear test methods with these new drafts was a much needed task. The new drafts will provide standard test methods for a wide variety of linear device families. Benefits from using standardized methods include reduced test time, increased consistency in obtaining test results, and more efficient comparisons of test data between different test laboratories. All of these will combine to improve the effectiveness of linear device test, which will in turn improve the reliability and performance of systems using linear devices.

APPENDIX A

This appendix includes copies of all 11 of the new series-4000 Linear Test Methods. These are unofficial copies and have been included for information purposes only. The official methods will be contained in the next revision of MIL-STD-883C.

METHOD 4001

OPERATIONAL AMPLIFIER PARAMETERS

1.0 PURPOSE. This method establishes the means for measuring input offset voltage and current, input bias current, common mode input voltage range, common mode rejection ratio, supply voltage rejection ratio, single ended voltage gain, output voltage swing, and input offset voltage adjustment range, power supply current, output short circuit current, channel separation, rise time, slew rate, noise and settling time for operational amplifier integrated circuits.

1.1 Definitions. The following definitions apply for the purpose of this test method.

1.1.1 Input Offset Voltage (V_{IO}). Input offset voltage is the dc voltage which must be applied between the input terminals through two equal resistances to force the quiescient dc output to zero or other specified level.

1.1.2 Input Offset Voltage Drift (DV_{IO}). Input offset voltage drift is the ratio of the change of input offset voltage to the change of circuit temperature. This typically generates a value expressed as microvolts per degree (°C).

$$DV_{IO} = \frac{\Delta V_{IO}}{\Delta T}$$

1.1.3 Input Offset Current (I_{IO}). The input offset current is the algebraic difference between the currents entering into the input terminals of a differential input amplifier.

$$I_{IO} = (+I_{IB}) - (-I_{IB})$$

1.1.4 Input Offset Current Drift (DI_{IO}). Input offset current drift is the ratio of the change in input offset current to the change of circuit temperature. This typically generates a value expressed as picoamps per degree (°C).

$$DI_{IO} = \frac{\Delta I_{IO}}{\Delta T}$$

1.1.5 Input Offset Voltage Adjustment Range ($V_{IO}(adj+)$, $V_{IO}(adj-)$). The input offset voltage adjustment ranges are the differences between the offset voltage (V_{IO}) measured with the voltage adjust terminals open circuited, and the offset voltage measured with the maximum positive or negative voltage attainable with the specified adjustment circuit

1.1.6 Input Bias Current ($+I_{IB}$, $-I_{IB}$). The input bias currents are the currents flowing into the inverting and non-inverting terminals of an operational amplifier.

1.1.7 Common Mode Input Voltage Range (V_{CM}). This is the range of common mode input voltage over which proper function of the operational amplifier is maintained. This parameter is guaranteed by testing CMRR to the limits of V_{CM}.

1.1.8 Common Mode Rejection Ratio (CMRR). The common mode rejection ratio is the ratio of the change in input common mode voltage to the resulting change in the input offset voltage. CMRR is usually expressed in decibels:

$$CMRR = 20 \text{ LOG } \left(\frac{\Delta V_{CM}}{\Delta V_{IO}} \right)$$

where ΔV_I = change in input offset voltage
ΔV_{CM} = change in common mode input voltage

1.1.9 Power Supply Rejection Ratio (PSRR). The power supply rejection ratio is the ratio of the change in input offset voltage, V_{IO}, to the corresponding change in power supply voltage usually expressed in microvolts per volt. PSRR may be tested either by shifting the voltage of one power supply with all remaining power supply voltages held constant, or by shifting both power supply voltages simultaneously. For the first method +PSSR and -PSSR are defined as follows:

$$+PSRR = \frac{\Delta V_{IO}}{\Delta(+V_{CC})} \qquad -V_{CC} = \text{constant}$$

$$-PSRR = \frac{\Delta V_{IO}}{\Delta(-V_{CC})} \qquad +V_{CC} = \text{constant}$$

For the second method, PSRR is defined as:

$$PSRR = \frac{\Delta V_{IO}}{\Delta(V_{CC})}$$

where ΔV_{CC} is obtained by shifting both power supplies, for example, from ± 20 V to ± 5 V.

1.1.10 Voltage Gain (A_V). The voltage gain (open loop) is the ratio of the change in the output voltage to the differential change in the input voltage. The input not connected to the signal source is at zero potential.

1.1.11 Output Voltage Swing (VOP). The maximum output voltage swing that can be achieved for a specified load without causing voltage limiting.

1.1.12 Channel Separation. This parameter is specified for dual and quad operational amplifiers integrated on the same semiconductor chip. It is a

measure of the amount of electrical coupling between amplifiers. When a signal is applied at the input of one amplifier, some portion will appear at the output of the other amplifier or amplifiers. Channel separation is measured in decibels.

1.1.13 Rise Time (t_R). The rise time of an operational amplifier is the time necessary for the output of the amplifier to rise from 10% of its output steady state value to 90% of its output steady state value for a specified input pulse.

1.1.14 Settling Time (t_s). The settling time for an operational amplifier is the time required for the amplifier output to change from some specified voltage level and to settle within a specified errorband of its final steady state value in response to the application of a specified input pulse.

1.1.15 Slew Rate (SR). Slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per microsecond.

1.1.16 Broadband Noise ($N_{I(BB)}$). Broadband noise is the true rms noise voltage including all frequency components measured at the output of the amplifier. Practical measurement of broadband noise requires specification of a minimum bandwidth over which the output noise voltage is measured.

1.1.17 Popcorn Noise ($N_{I(PC)}$). Popcorn noise consists of randomly occurring bursts of noise across the broadband range. $N_{I(PC)}$ is expressed in μV_{peak} referenced to the amplifier input.

1.1.18 Input Noise Voltage Density (V_n). The input noise voltage density is the rms noise voltage in a 1 Hz band centered on a specified frequency.

V_n is expressed in $nV/\sqrt{Hz}$ referenced to the amplifier input.

1.1.19 Input Noise Current Density (I_n). The input noise current density is the rms noise current in a 1 Hz band centered on a specified frequency.

I_n is expressed in $nA/\sqrt{Hz}$ referenced to the amplifier input.

2.0 APPARATUS. The apparatus shall include the necessary equipment needed to implement the test circuits shown in figures 1, 2, 4, 5, 7 and 8. If the optional integrated capacitor method is used to measure leakage currents, then additional circuit components needed to implement the setup in figure 3 may be required. Operational amplifier bias power supplies not shown in the figures will be as specified in the procurement document.

2.1 DC Voltmeters (VM1, VM2). The dc voltmeters shown in figures 1 and 3 shall have input impedances sufficiently high as not to load the circuit under test. Accuracy shall be such that it will have less than ten percent effect on the tolerance specified for the circuit tested. For example, if a reading should be 0 $\pm$ 0.1V to be acceptable for the circuit tested, the voltmeter shall be accurate to within $\pm$0.01 V.

2.2 Bias Power Supplies. Device power supplies will be programmable to provide $+V_{CC}$ and $-V_{CC}$ voltages at nominal levels specified for the device in test. The supplies shall be accurate to 0.1%.

2.3 Stabilization Networks. For all test circuits, stabilization shall be appropriate to stabilize the circuit to prevent oscillation. If a maximum peak-to-peak level of oscillation is specified in the procurement document, then an oscillation detector at the device output shall be used to guarantee that peak-to-peak noise above this level shall be cause for device failure.

2.4 Resistor and Capacitor Networks. The value of the resistors not specified in the appropriate test circuit will be provided by the procurement document. Alternatively, in figure 1, resistor R_2 shall be chosen to have a value no larger than the nominal input impedance nor less than a value which will load the amplifier ($10*Z_O$). R_1 should be chosen such that $R_2/R_1 = 1000$ or some other convenient scale factor. Resistors used for setting loop gain shall be within 0.1% or better precision. All other resistors shall be within 1% of the specified value. The accuracy of the capacitors used in all test circuits (except figure 3) shall be ±10% unless otherwise specified in the procurement document.

2.5 Operational Amplifier. The nulling operational amplifier, A1, in figures 1, 2 and 3 amplifies and inverts error voltages at the output of the DUT. Recommended type is M38510/135 or superior low offset precision operational amplifier.

2.6 Output Voltage Supply (VS_1). The output voltage supply in figure 1 will be programmable to force a specific output voltage on the amplifier under test. The supply must have an accuracy of 0.01%.

2.7 Programmable Load Resistor (R_L). The load resistor in figures 1 and 2 must be programmable or switch selectable to simulate any load required for the amplifier under test. The values needed will be obtained from the procurement document and may include an open circuit condition. Resistors will be accurate to within 1.0%.

2.8 Integrating Capacitor. The integrating capacitor used in the low leakage test circuit shown in figure 3 must have a dielectric resistance sufficiently high as to contribute less than 10% to measured leakage. In addition the capacitor should have low dielectric absorbtion.

2.9 Pulse Generator (VS_2). The pulse generator used in figures 4 and 5 shall have a rise time and repetition rate sufficient to perform the tests described in sections 3.16 to 3.18 on the amplifier under test. The pulse generator must also have an output impedance of 50Ω.

2.10 Pulse Shaping Network. Some test circuits may require an RC network between the pulse generator and the amplifier under test for matching purposes as shown in figures 4 and 5. This network must be specified in the procurement document.

2.11 Oscilloscope (OSC). The oscilloscope or alternate time measuring system shown in figures 4 and 5 shall have sufficient bandwidth to measure timing parameters equivalent to those in the specification with an accuracy of 1%. The oscilloscope shall have an input impedance of 1 MΩ or greater. Some device types may require the use of a FET probe or other high impendance buffer device to minimize distortion of output waveform.

2.12 AC Voltmeter (VM3). An AC voltmeter is required to make noise measurements using the circuit in figure 7. For broadband noise VM3 must read true rms voltage. Popcorn noise requires a peak reading voltmeter or equivalent apparatus. VM3 must have a minimum bandwidth of 10 Hz to 15 kHz.

2.13 Noise Analyzer Amplifier and Filter Units. The test circuit in figure 8 requires both an amplifier and filter unit. The characteristics of these units are described in more detail in sections 3.21 and 3.22.

3.0 PROCEDURE. The approach used to measure operational amplifier static parameters is the nulling amplifier method illustrated in figure 1. An alternative approach, the integrating capacitor method, shown in figure 3, is also described for measurement of very low currents. Table 1 summarizes the test conditions, measurements and equations for all static tests. Circuits and diagrams needed to measure the dynamic performance of operational amplifiers are shown in figures 4 to 8. Dynamic parameters are measured using the test circuits shown in figures 4 and 5. Figures 7 and 8 show test circuits used to measure the noise characteristics of the amplifier under test. The test conditions, measurements and equations for these parameters are included on the test circuit diagrams and in the following text instead of Table 1.

3.1 Input Offset Voltage (V_{IO}). Input offset voltage is tested with switches S_1 and S_2 closed. V_{S1} is set to required condition. The nulling amplifier output, E_O, is measured and V_{IO} determined from the equation:

$$V_{IO} = \frac{R_1}{R_2} (E_O) \qquad \mu V$$

3.2 Input Offset Voltage Adjustment Range ($V_{IO}(adj)$). The input offset voltage adjust is determined by measuring input offset voltage (V_{IO}) using the procedure in section 3.1. Maximimum positive and negative adjust ranges are measured. Maximium applied voltages at the adjust terminals will be specified in the procurement document. Two values are measured. $V_{IO}(+)$ is determined by measuring with the maximum condition applied to the positive adjust terminal. $V_{IO}(-)$ is found similarly except the maximum is applied to the negative terminal. Then:

$$V_{IO}(adj+) = V_{IO} - V_{IO}(+) \qquad V$$

$$V_{IO}(adj-) = V_{IO} - V_{IO}(-) \qquad V$$

where V_{IO} is the input offset voltage measured in section 3.1.

3.3 Input Offset Voltage Drift (DV_{IO}). Measurement of V_{IO1} is made at temperature T_1 as described in section 3.1, and a second measurement of V_{IO2} is made at the second temperature (T_2). DV_{IO} is then calculated as:

$$DV_{IO} = \frac{V_{IO2} - V_{IO1}}{T_2 - T_1} \qquad \mu V/°C$$

3.4 Input Offset Current (I_{IO}). The test circuit is initially configured with the load resistor removed, VS_1 programmed to required conditions, and switches S_1 and S_2 both closed. VM2 is used to measure the output voltage, E_3. Switches S_1 and S_2 are then both opened and output voltage E_4 is measured. I_{IO} is then calculated using the following equation:

$$I_{IO} = \frac{R_1}{R_2}\left(\frac{E_3 - E_4}{R_3}\right) \qquad \mu A$$

3.5 Input Offset Current Drift (DI_{IO}). Measurement of I_{IO1} is made at temperature T_1 and I_{IO2} at temperature T_2 as in section 3.4. DI_{IO} is then calculated as:

$$DI_{IO} = \frac{I_{IO2} - I_{IO1}}{T_2 - T_1} \qquad \mu A/°C$$

3.6 Input Bias Currents ($+I_{IB}$, $-I_{IB}$). Input bias current is tested with load resistor R_L, and power supply VS_1 programmed to required condition. The nulling amplifier output voltage E_0 is first obtained with switches S_1 and S_2 closed. Output voltage E_5 is then measured with switch S_1 closed and S_2 open and output voltage E_6 is measured with switch S_1 open and S_2 closed. The input bias currents are calculated as:

$$+I_{IB} = \left(\frac{E_5 - E_0}{R_3}\right)\left(\frac{R_1}{R_2} + 1\right) \qquad \mu A$$

$$-I_{IB} = \left(\frac{E_0 - E_6}{R_3}\right)\left(\frac{R_1}{R_2} + 1\right) \qquad \mu A$$

3.7 Voltage Gain (A_V). Voltage gain of the amplifier is determined by making two measurements with the output voltage and load resistance set as specified in the procurement document. The power supply VS_1 is programmed to the specified output voltage level, V_{O1} and resistor R_L is set to the value specified. VM2 is used to measure voltage E_7 for this condition. VS_1 is then set to the second output voltage level, V_{O2} and E_8 is measured with VM2. The voltage gain is obtained from the equation:

$$A_V = \frac{V_{O2} - V_{O1}}{\Delta E} \qquad V/V$$

$$\text{where} \quad \Delta E = \frac{E_8 - E_7}{(R_2/R_1)}$$

3.8 Output Voltage Swing (VOP). Output voltage swing (peak-to-peak) is tested by driving the output voltage of the amplifier to levels specified in the procurement document. The test determines whether the operational amplifier will reach the specified positive and negative output voltage

levels, +VOP and -VOP, for the device. The test is accomplished in the circuit of figure 1 by driving the input of the nulling amplifier with power supply VS_1 through resistor R_5 set equal to R_4. The drive levels V_{O3} and V_{O4} will be equal in magnitude and opposite in polarity to the specified operational amplifier outputs. VM1 is used to measure the output voltages, E_9 and E_{10}. Switches S_1 and S_2 are closed for this test. Load resistor R_L is set as specified in the procurement document. The output voltage swing is defined by:

$$+VOP = E_9, \quad \text{and} \quad -VOP = E_{10}$$

3.9 Common Mode Rejection Ratio (CMRR). CMRR is determined from two measurements of the input offset voltage (V_{IO}) with positive and negative common mode voltage (V_{CM}) applied. Common mode conditions are achieved by algebraically subtracting V_{CM} from each supply. For example, if V_{CM} = -11 volts, then +VCC = 15V - (-11V) = +26V and -VCC = -15V - (-11V) = -4V. To center the voltage swing at the input of the nulling amplifier at zero volts, voltage equal to the common mode voltage and opposite in polarity is applied at VS_1. Let E_{11} be the voltage measured at E_o with VS_1 set at the positive common mode voltage, V_{CM1}, and E_{12} the voltage at E_o with VS_1 set at the negative common mode voltage, V_{CM2}, then:

$$CMRR = 20*LOG \left(\frac{V_{CM2} - V_{CM1}}{R_1/R_2(E_{12} - E_{11})} \right) \quad \text{decibels}$$

3.10 Common Mode Input Voltage Range (V_{CM}). This test shall be an implied measurement. The maximum common mode input voltage specified for the amplifier shall be used in making the common mode rejection ratio test of section 3.9.

3.11 Power Supply Rejection Ratio (+PSRR, -PSRR). +PSRR and -PSRR are determined by measuring the shift in the input offset voltage occurring when one power supply is shifted from nominal level while the other is maintained at a constant level. This requires two measured values of V_{IO}. These values can be obtained by shifting the power supply once and using the value of V_{IO} obtained under these conditions along with the input offset voltage measured in section 3.1. Alternatively, the power supply may be shifted above and below the nominal level with V_{IO} measured at each condition. For example, +PSRR may be determined from measurements of V_{IO} made with +VCC at 20V and 10V while -VCC is maintained at -15V. The measured values are scaled to give a result in microvolts change of V_{IO} per volt change in power supply voltage. The equation for +PSRR is:

$$+PSRR = \frac{(R_2/R_1)(E_{14} - E_{13})}{\Delta+V_{CC}} \quad \mu V/V$$

where: ΔV_{CC} = Change in supply voltage
$E_{13} = E_o$ for first +VCC level
$E_{14} = E_o$ for second +VCC level

Similarly,

$$-PSRR = \frac{(R_2/R_1)(E_{16} - E_{15})}{\Delta(-V_{CC})} \qquad \mu V/V$$

where: ΔV_{CC} = Change in supply voltage
$E_{15} = E_o$ for first -VCC level
$E_{16} = E_o$ for second -VCC level

3.12 Power Supply Current (ICC). Power supply current shall be measured using method 3005.1 of MIL-STD-883C for all device power supplies.

3.13 Output Short Circuit Current (I_{OS}). Short circuit current will be measured using the procedures outlined in method 3011.1 of MIL-STD-883C. Two such measurements are required. $I_{OS}(+)$ is measured with the amplifier output at a specified positive voltage, and $I_{OS}(-)$ is measured with a specified negative voltage on the amplifier output. The duration of the short circuit will be specified in the procurement document.

3.14 Channel Separation (CS). Channel separation for dual and quad operational amplifiers is tested in the circuit of figure 2. CS is tested for each amplifier with respect to all other amplifiers. Thus two tests are performed for a dual amplifier and 12 for a quad operational amplifier. The test circuit of figure 2 is applicable to both dual and quad amplifiers. The connection shown is for measurement of amplifier B output sensitivity with respect to a signal applied to the input of amplifier A. Amplifiers C and D, if present, are connected as shown for unit gain. The gain setting resistors, R_6 and R_7, for amplifier A will be as specified in the procurement document if required. For many devices, R_6 will be omitted and R_7 will be replaced by a direct connection from the inverting input to the output resulting in a gain of 1 for the driven amplifier.

The test procedure is as follows: Two levels of input voltage V_{IN}, for example, ±10 V, are applied successively and output voltages E_{17} and E_{18} measured by VM2. CS is calculated by comparing the change in output voltage of the driven amplifier with the voltage change at the output of the passive amplifier:

$$CS = 20*LOG\left(\frac{(\Delta V_{IN})A_V}{(E_{18} - E_{17})/A_L}\right) \qquad \text{decibels}$$

where: ΔV_{IN} is the change in input voltage
A_V is the voltage gain of the driven amplifier = R_2/R_1
$E_{18} - E_{17}$ is the change in output voltage corresponding to ΔV_{IN}
A_L is the loop gain for the nulling amplifier circuit = 1000

3.15 Input Bias Current ($+I_{IB}$, $-I_{IB}$) by the Integrating Capacitor Test Method. The integrating capacitor method may be used for the measurement of very low input bias currents. Two alternative approaches to the integrating capacitor method are shown in the test circuits of figures 3(a) and 3(b).

Both approaches rely on the basic relationship of the current to the rate of change of voltage when a capacitor is charged by a constant current:

$$I = C \frac{\Delta E}{\Delta t} \quad \mu A$$

where: I = a constant charging current
C = capacitance of capacitor
$\Delta E/\Delta t$ = charging rate

The method defined by the circuit of figure 3(a) is suitable for measurement of any small current, I_X, which may be sourced or sunk at point A. To measure the input bias current, $+I_{IB}$ or $-I_{IB}$, at the input of an operational amplifier in test, the device is biased at nominal supply levels and operated in open loop condition. The input to be tested is connected to point A in the test circuit and the other input is connected to zero volts. Voltage E_{o1} is measured initially with switch S closed. The switch is then opened and E_{o2} measured after t seconds. Then:

$$I_X = \frac{-(E_{o2} - E_{o1})}{t} * C \quad \mu A$$

The method of figure 3(b) is a variation of the nulling amplifier circuit. To obtain $-I_{IB}$, output voltage E_{o1} is measured with switches S_1 and S_2 closed. S_1 is then opened and after t seconds E_{o2} is measured. Then:

$$-I_{IB} = \frac{-(E_{o2} - E_{o1})}{t} * C_1 * (49.9/R_F)$$

To obtain $+I_{IB}$, E_{o1}, is again measured with the switches closed, switch S_2 is opened and after t seconds E_{o3} is measured. Then:

$$+I_{IB} = \frac{-(E_{o3} - E_{o1})}{t} * C_1 * (49.9/R_F)$$

Input offset current may be calculated from $+I_{IB}$ and $-I_{IB}$,

$$I_{IO} = +I_{IB} - (-I_{IB})$$

3.16 Settling Time (t_s). Settling time is measured in the circuit of figure 4. A pulse of specified amplitude and rise time much faster than the settling time of the amplifier in test is applied to the input. The input and output voltages are compared at the output of the FET voltage follower stage using an oscilloscope or alternate apparatus. The ratio of input and feedback resistors, R_1 and R_2, will be specified in the procurement document and will generally be 1 to 1. The scaling factor for the voltage follower input R_3/R_4 may be specified in the procurement document or chosen for convenience in

making an accurate measurement. The waveform is observed as illustrated in figure 4 with δV adjusted for the voltage follower divider ratio if necessary.

Alternate settling time: Using the circuit shown in figure 5, a specified input pulse is applied to the device under test. The output waveform is observed on an oscilloscope as illustrated in figure 6. V_1 is a specified level and V_2 is the final voltage after settling. The settling time is determined as the time for the output to fall from V_1 and settle within the specified error band (obtqained from the procurement document) of V_2.

3.17 Rise Time (t_r). Rise time is measured using the test circuit shown in figure 5. An input pulse of rise time and amplitude as specified in the procurement document is applied and the output waveform is observed on the oscilloscope. Pulse duration and repetition rate are set to enable easy observation of output waveform. Rise times are measured between the 10% and 90% points on the output waveform as shown in figure 6.

3.18 Slew Rate (SR). Slew rate is also measured using the test circuit in figure 5. An input pulse of rise time and amplitude as specified in the procurement document is applied to the amplifier. This pulse will cause the output to slew between specified voltages. The output waveform is observed on the oscilloscope and SR(+) and SR(-) calculated for rising and falling waveforms as indicated in figure 6.

3.19 Broadband Noise ($N_{I(BB)}$). Broadband noise is measured in the circuit of figure 7 with switch S1 closed. E_0 is measured using a true rms voltmeter. All noise measurements are referred to the input. It is assumed that all noise sources within the amplifier in test are set to zero and that the noise measured at the output is input noise multiplied by the circuit gain.

3.20 Popcorn Noise ($N_{I(PC)}$). Popcorn noise is measured in the circuit of figure 7 with switch S1 closed. E_0 is measured using a peak reading voltmeter or equivalent apparatus. The duration of the measurement and the resistance of resistors R_S will be as specified in the procurement document.

3.21 Input Noise Voltage Density (V_n). V_n is measured in the circuit of figure 8. The noise analyzer amplifier unit shown is a variable gain low noise amplifier; the noise analyzer filter unit consists of a true rms voltmeter with selectable narrow band input filters. Ideally noise is measured over a 1 Hz bandwidth located at the center of the amplifier bandwidth. This method gives a measured voltage density since the square root of the bandwidth equals 1. In general, the noise analyzer filter unit bandpass filter will have a bandwidth of greater than 1 Hz. To obtain the correct measured noise voltage referenced to the input of the operational amplifier, the voltmeter reading must be corrected for gain and bandwidth.

$$E_m = \frac{E_t}{A\sqrt{NBW}} \qquad V_{RMS}/\sqrt{Hz}$$

where E_t = rms voltage reading of noise analyzer filter unit.

A = total gain of operational amplifier and noise analyzer amplifier unit.

NBW = noise bandwidth of bandpass filter at the frequency of measurement.

E_m = measured noise voltage density.

The square of the measured noise voltage density, E_m, is the sum of the squares of the actual input noise voltage density, the noise voltage density of the input current across the input resistor, and the input resistor thermal noise density.

$$E_m^2 = V_n^2 + R_s^2 * I_n^2 + 4KTR_s$$

where V_n = input noise voltage density.

I_n = input noise current density.

4KT = (4)(Boltzman's constant)(°K)

$= 1.64*10^{-20}$ at 25 °C.

R_s = source resistance = R_1 in figure 8.

The value of $R_S = R_1$ of figure 8 is chosen so that the contribution of the input current density is negligible. Then:

$$V_n^2 = E_m^2 - \left(1.64*10^{-20}\right) R_s \qquad (V_{RMS})^2$$

The resistor values R_1 and R_2 may be set in the procurement document. As an example, to obtain V_n, resistors R_1 and R_2 are set to 50Ω and 10 kΩ respectively for an operational amplifier gain of 200. The gain of the noise analyzer amplifier is set to make the total gain to the input of the filter equal to 10,000. The noise voltage, E_t, is measured using the appropriate filter in the noise analyzer filter unit and corrected for amplification and filter bandwidth as above to obtain E_m. V_n is then calculated from E_m using the equation above.

3.22 Input Noise Current Density (I_n). Noise current density is tested in the circuit of figure 8 using the same apparatus as for the noise voltage measurement. Noise voltage is first obtained from the procedure of Section 3.21. The measurement is then repeated with the value of resistor $R_1 = R_S$ made large enough that the current contribution to the total noise voltage is significant. Then:

$$I_n^2 = \frac{1}{R_s^2}\left(E_m^2 - V_n - 1.64*10^{-20}* R_s\right) \qquad A_2/Hz$$

where all variables are as defined in Section 3.19.

The resistor values R_1 and R_2 may be set in the procurement document. As an example for R_1 = 10 kΩ and $R2$ = 2.0 MΩ and gain of the noise analyzer amplifier unit set to give a circuit gain of 10,000 then:

$$I_n^2 = \left(E_m^2 - V_n - 1.64*10^{-15}\right)*10^{-10} \qquad A_2/Hz$$

where all variables are as defined in Section 3.19.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document.

a. $+V_{CC}$ and $-V_{CC}$ for each test.
b. Maximum and minimum conditions applied to the voltage. adjust terminal for V_{IO}(adj) tests.
c. R_L for VOP, CMRR and A_V tests.
d. V_O levels for CMRR and A_V tests.
e. V_{CM} values required for common mode tests.
f. $\Delta(+V_{CC})$ and $\Delta(-V_{CC})$ for PSRR test.
g. V_O minimum and maximum for VOP test.
h. V_O level for $I_{OS}(-)$ and $I_{OS}(+)$ measurements.
i. Maximum duration for I_{OS} tests.
h. Resistor values for R_1, R_2, R_3 in the test circuit of figure 1.
i. Input voltage levels for the channel separation test
j Resistor values for R_6 and R_7 in the test circuit of figure 2 if required.
k. Input pulse waveforms tor each dynamic test.
l. Any RC waveshaping network required at the input to the DUT.
m. Starting and ending voltages for dynamic tests and percent. bounds for settling time.
n. All load capacitors and resistors used in the tests.
o. Limit value for each parameter tested.
p. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.

PARAMETER	SWITCHES S_1	SWITCHES S_2	LOAD RESISTOR R_L	OUTPUT VOLTAGE VS_1	MEASUREMENT METER	MEASUREMENT VALUE	EQUATION	UNIT	NOTES
V_{IO}	CLOSED	CLOSED	OPEN	A_D	VM2	E_0	$V_{IO} = (R_1/R_2) * (E_0)$	VOLT	SEE NOTE 1
$V_{IO}(adj)$	CLOSED CLOSED	CLOSED CLOSED	OPEN OPEN	A_D A_D	VM2 VM2	E_1 E_2	$V_{IO}(adj+) = (E_0 - E_1)/A_D$ $V_{IO}(adj-) = (E_0 - E_2)/A_D$	VOLT VOLT	SEE NOTE 2
I_{IO}	CLOSED OPEN	CLOSED OPEN	OPEN OPEN	A_D A_D	VM2 VM2	E_3 E_4	$I_{IO} = \frac{R_1}{R_2}\left(\frac{E_3 - E_4}{R_3}\right)$	AMPS	SEE NOTE 1
I_{IB}	CLOSED OPEN	OPEN CLOSED	OPEN OPEN	A_D A_D	VM2 VM2	E_5 E_6	$+I_{IB} = \left(\frac{R_1}{R_2} + 1\right)\left(\frac{E_5 - E_0}{R_3}\right)$ $-I_{IB} = \left(\frac{R_1}{R_2} + 1\right)\left(\frac{E_0 - E_6}{R_3}\right)$	AMPS	SEE NOTE 1
A_V	CLOSED CLOSED	CLOSED CLOSED	R_L R_L	V_{O1} V_{O2}	VM2 VM2	E_7 E_8	$A_V = \left(\frac{V_{O2} - V_{O1}}{\Delta E}\right)$ $\Delta E = \frac{E_8 - E_7}{(R_2/R_1)}$	NONE	
VOP	CLOSED CLOSED	CLOSED CLOSED	R_L R_L	V_{O3} V_{O4}	VM1 VM1	E_9 E_{10}	$+VOP = E_9$ $-VOP = E_{10}$	VOLT	
CMRR	CLOSED CLOSED	CLOSED CLOSED	OPEN OPEN	V_{O5} V_{O6}	VM2 VM2	E_{11} E_{12}	$CMRR = 20*LOG\left(\frac{V_{O6} - V_{O5}}{\Delta E}\right)$ $\Delta E = \frac{E_{12} - E_{11}}{(R_2/R_1)}$	dB	

Table 1. Equations For Static Operational Amplifier Tests

PARAMETER	SWITCHES S_1	SWITCHES S_2	LOAD RESISTOR R_L	OUTPUT VOLTAGE VS_1	MEASUREMENT METER	MEASUREMENT VALUE	EQUATION	UNIT	NOTES
+PSRR	CLOSED	CLOSED	OPEN	A_D	VM2	E_{13}	$PSRR = \frac{E_{14} - E_{13}}{(R_2/R_1) * \Delta VCC}$	$\frac{\mu V}{V}$	SEE NOTE 3
	CLOSED	CLOSED	OPEN	A_D	VM2	E_{14}			
-PSRR	CLOSED	CLOSED	OPEN	A_D	VM2	E_{15}	$PSRR = \frac{E_{14} - E_{13}}{(R_2/R_1) * \Delta VCC}$	$\frac{\mu V}{V}$	SEE NOTE 4
	CLOSED	CLOSED	OPEN	A_D	VM2	E_{16}			
CS	----	----	R_L	---	VM2	E_{17}	$CS = 20*LOG \left(\frac{(\Delta V_{IN})*(R_2/R_1)}{(E_{18} - E_{17})/A_L} \right)$	dB	SEE FIG. 2
	----	----	R_L	---	VM2	E_{18}			SEE NOTE 5

NOTES:
1. If using Integrated Capacitor Method, refer to equations in section 3.13
2. E_1 measured with maximum voltage applied to adjust terminal, E_2 measured with minimum voltage applied to adjust terminal
3. E_{13} measured with +VCC at nominal level, E_{14} measured with +VCC at adjusted level
4. E_{15} measured with -VCC at nominal level, E_{16} measured with -VCC at adjusted level
5. A_L is loop gain for nulling amplifier in figure 2
6. Input Voltage (V_{qi}) for each test will be specified in the procurement document
7. A_D = (R2/R1) + 1

Table 1. Equations For Static Operational Amplifier Tests (cont)

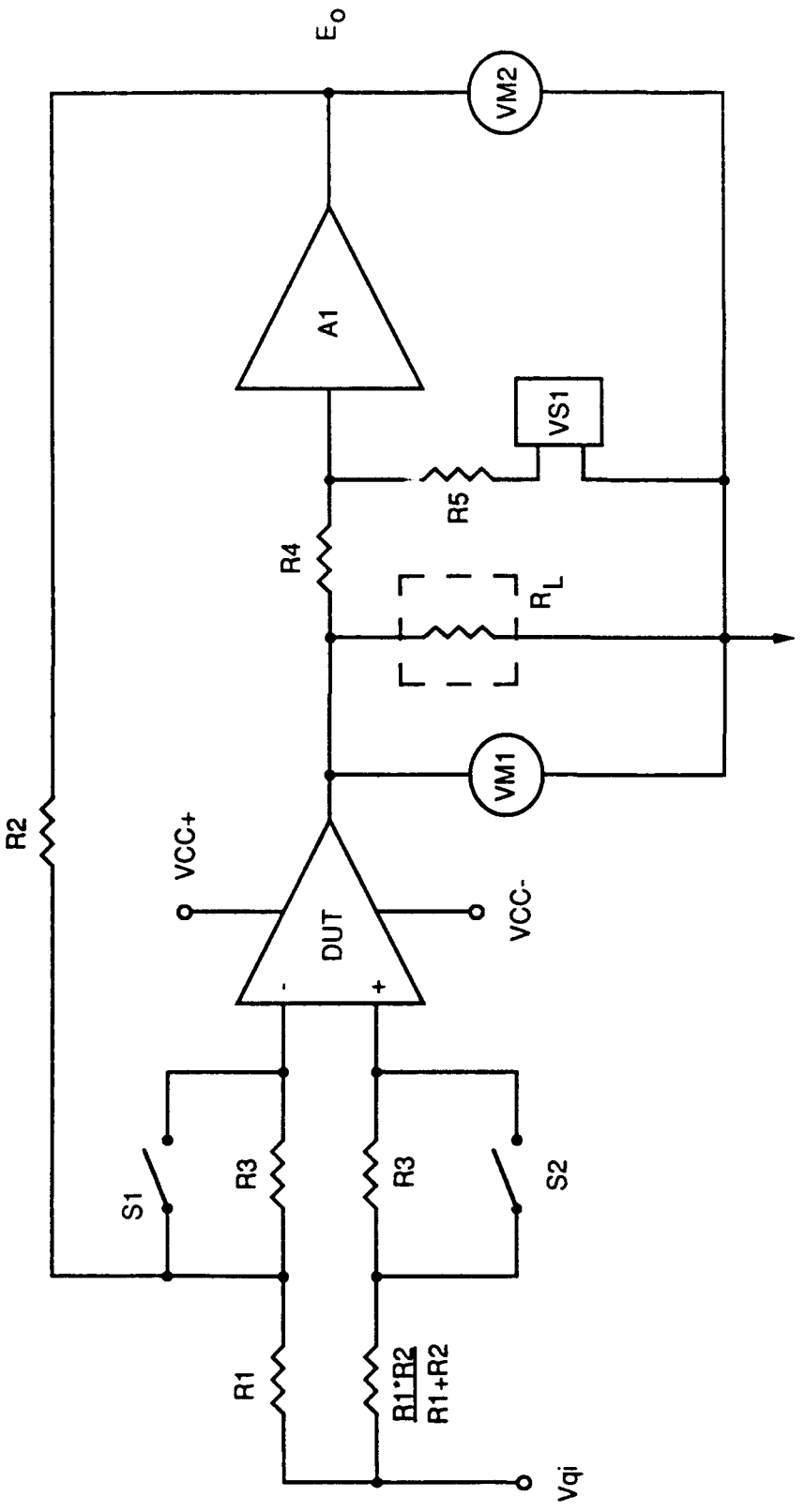
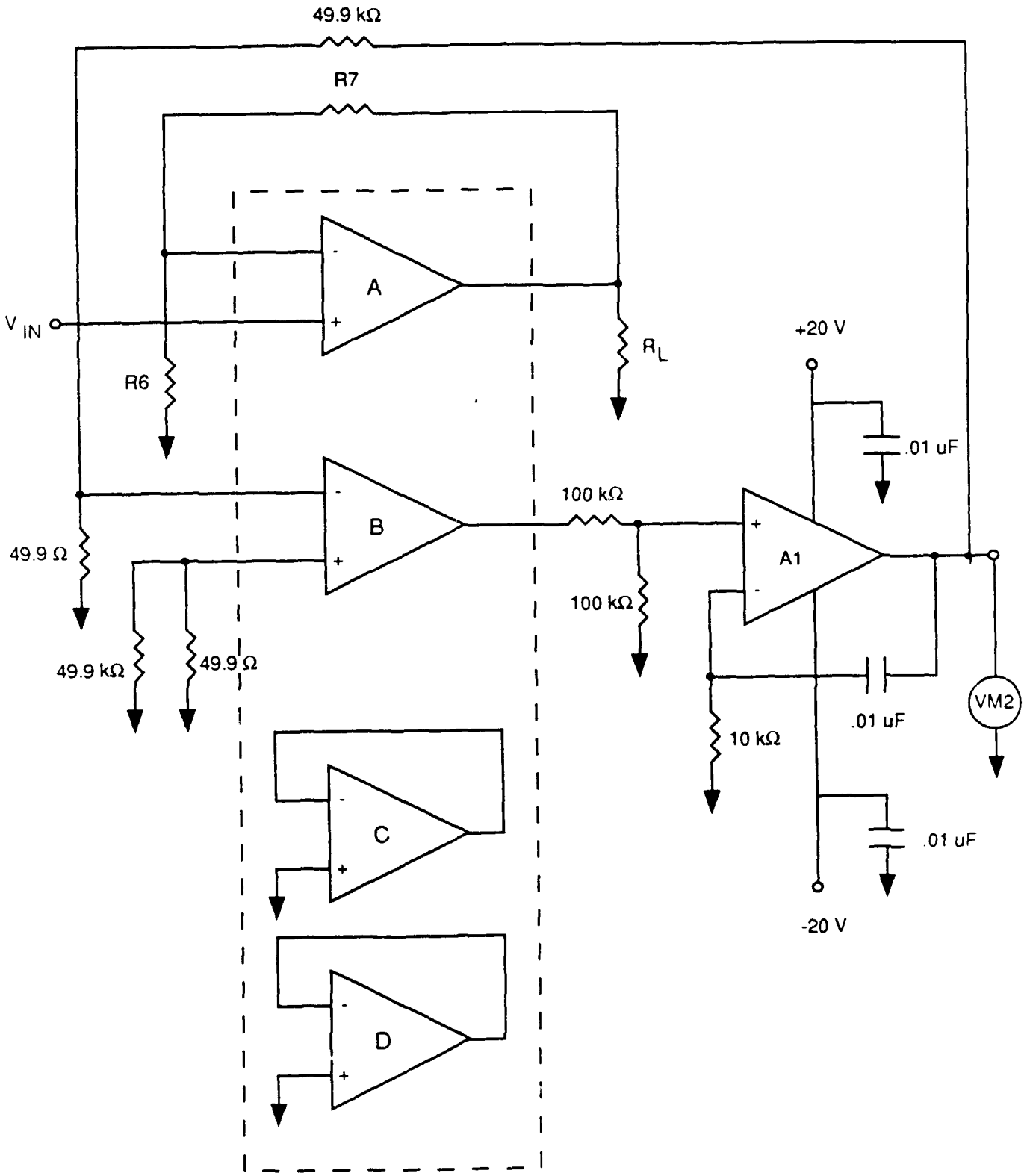


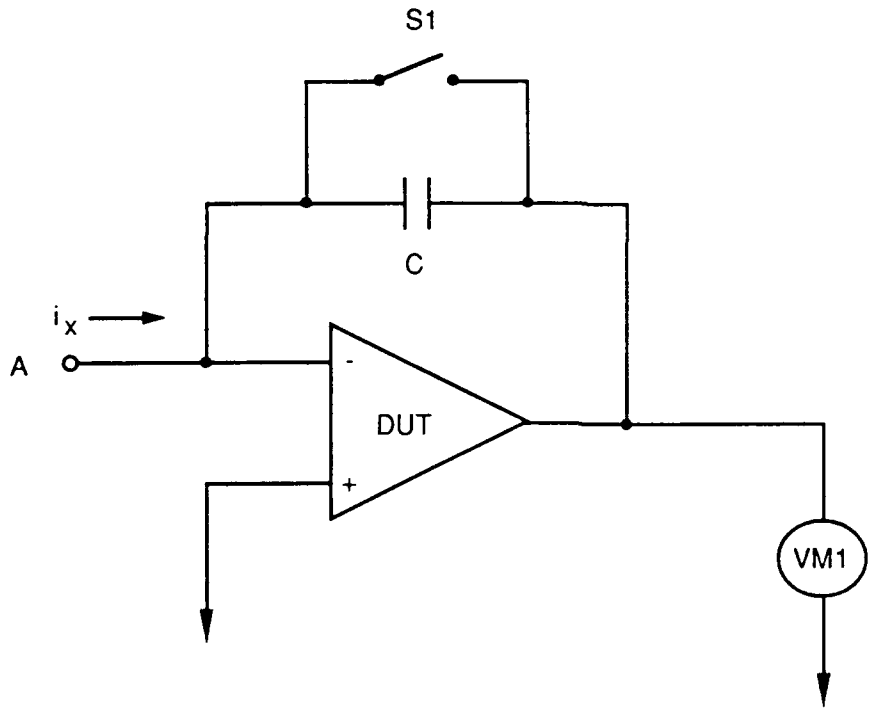
Figure 1. Operational Amplifier Test Circuit



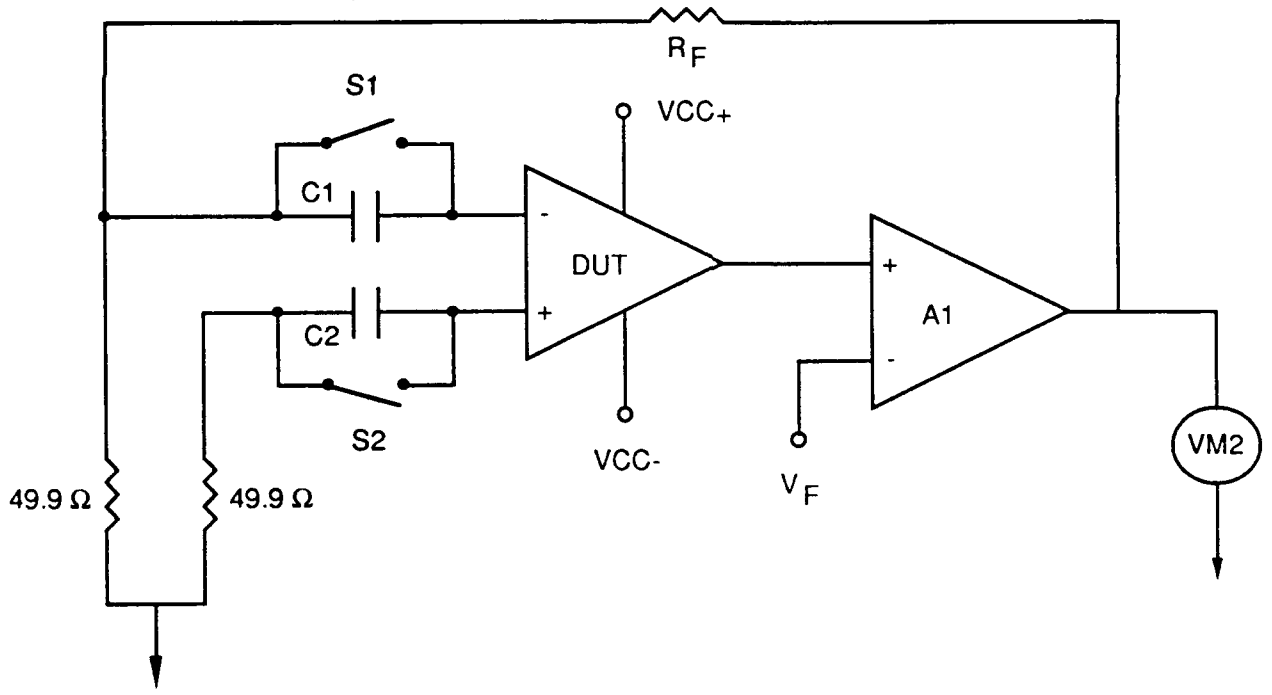
Notes: 1. All resistors +/- 0.1% tolerance, all capacitors +/- 10% tolerance

2. The nulling amplifier shall be MIL-M-38510/135 or similar. Saturation of the amplifier is not allowed

Figure 2. Channel Separation Test Circuit

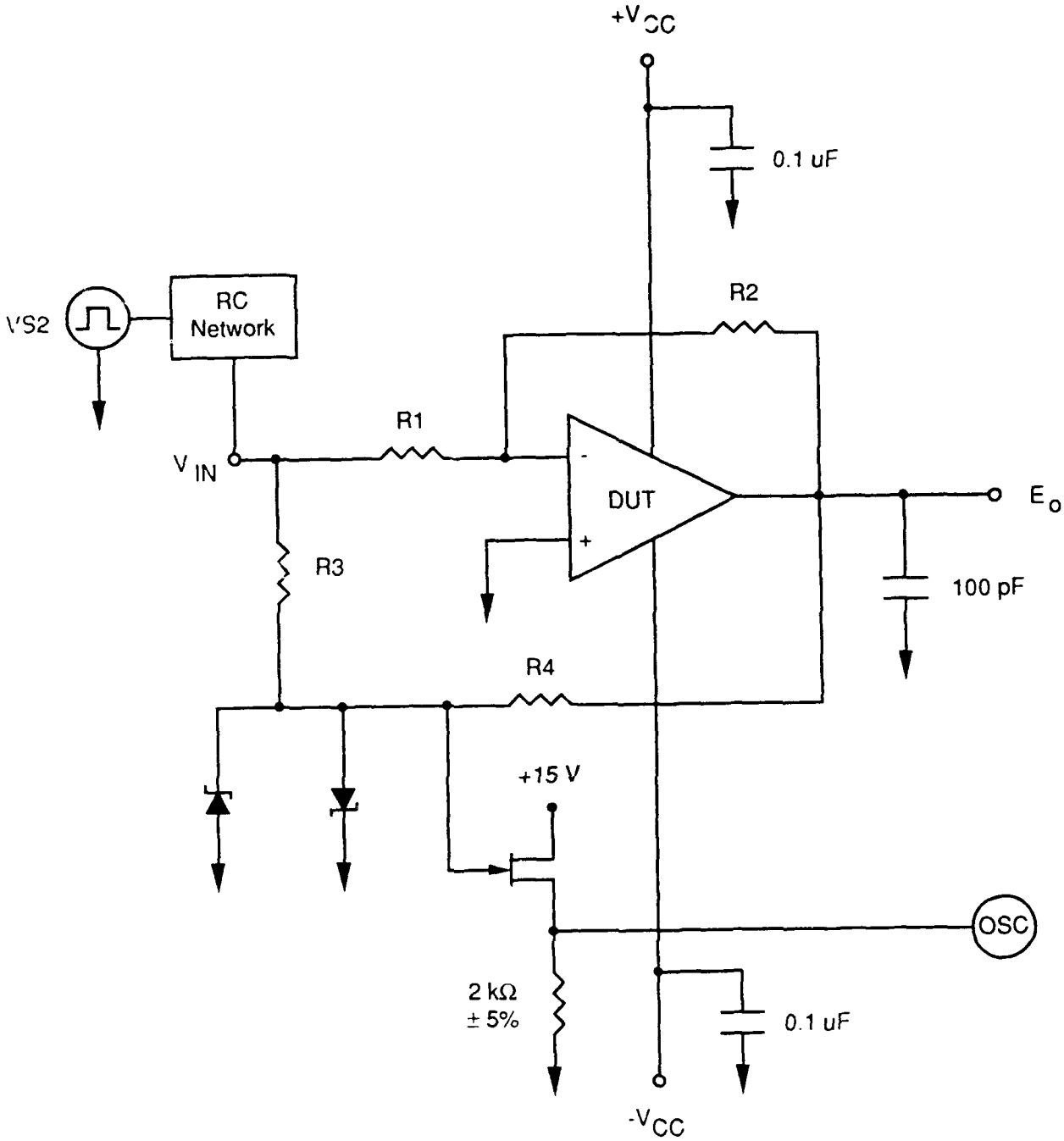


(A)



(B)

Figure 3. Test Circuits for Low Leakage Current Amplifiers



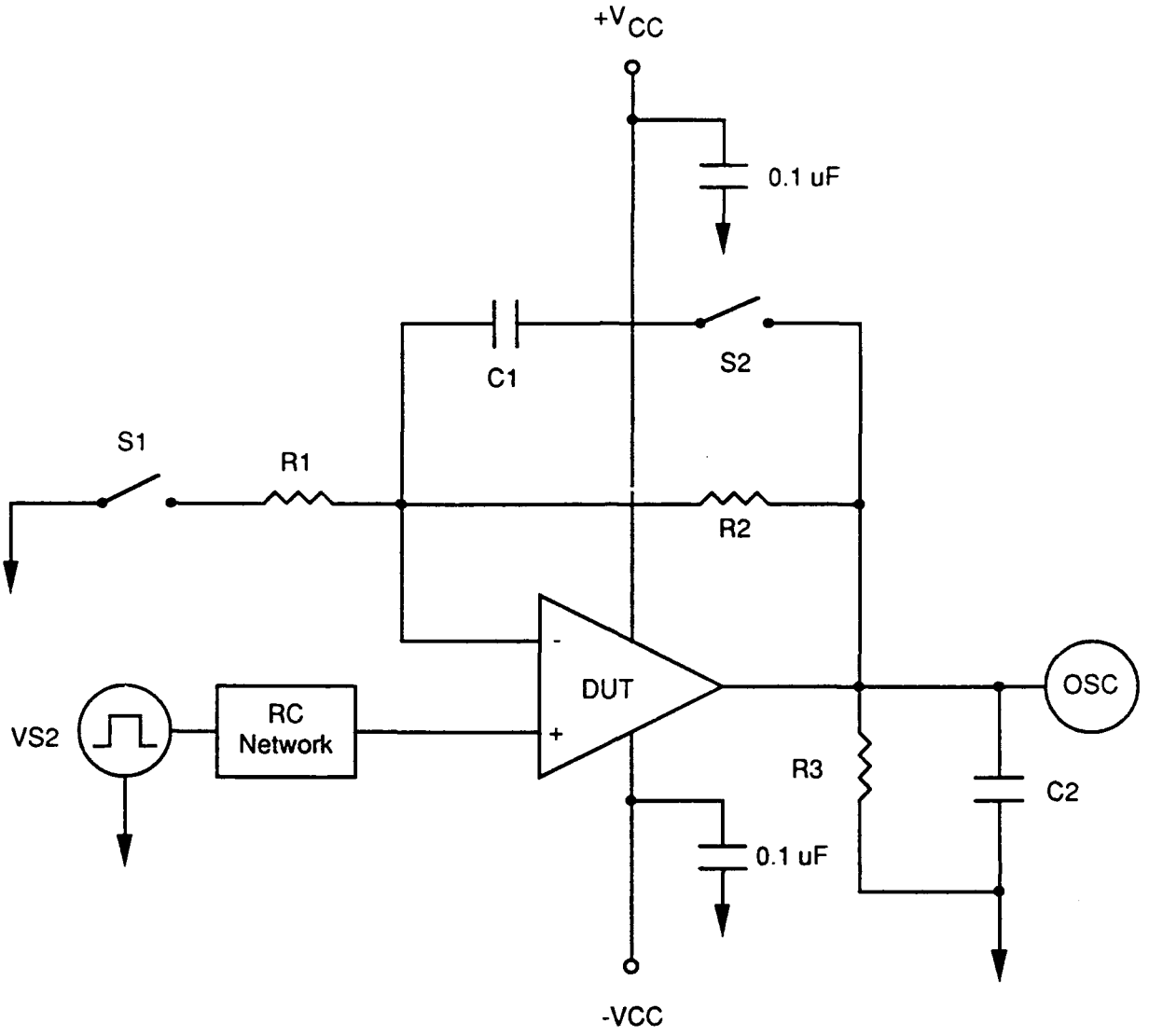
Notes: 1. Resistors have ±0.1% tolerance, capacitors have ±10% tolerance unless otherwise specified

2. Precaution shall be taken to prevent damage to DUT during insertion.

3. Settling time is the interval during which the summing made is not nulled to within ± 0.5ΔV

4 Diodes are 1N5711 Schottky diodes

Figure 4. Operational Amplifier Settling Time Test Circuit



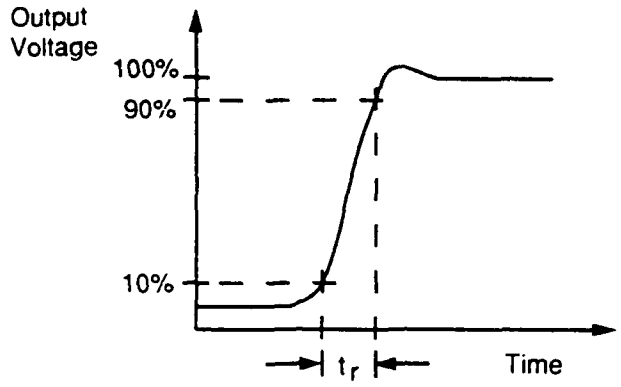
Operational Amplifier Dynamic Parameter Test Circuit

Circuit Gain	Switch S1	Switch S2
Unity	OPEN	CLOSED
R2/R1 +1	CLOSED	OPEN

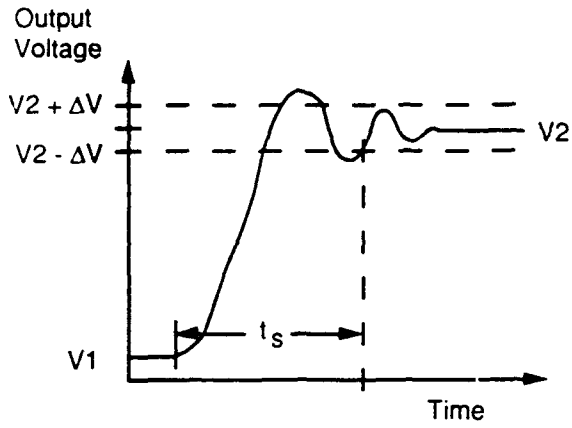
Switch Positions For Dynamic Tests

Notes: 1. C1 not required for some part types

Figure 5. Operational Amplifier Dynamic Test Circuit

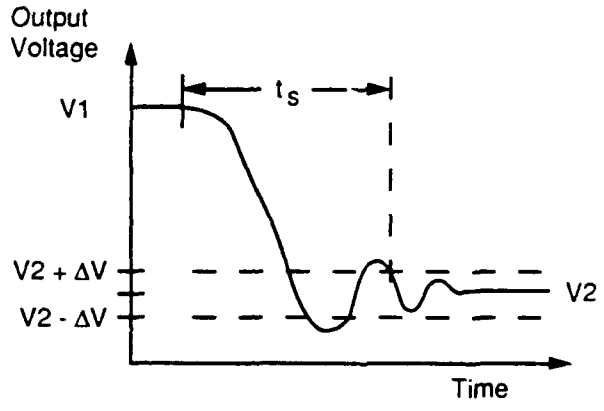


Rise Time (tr) Waveform



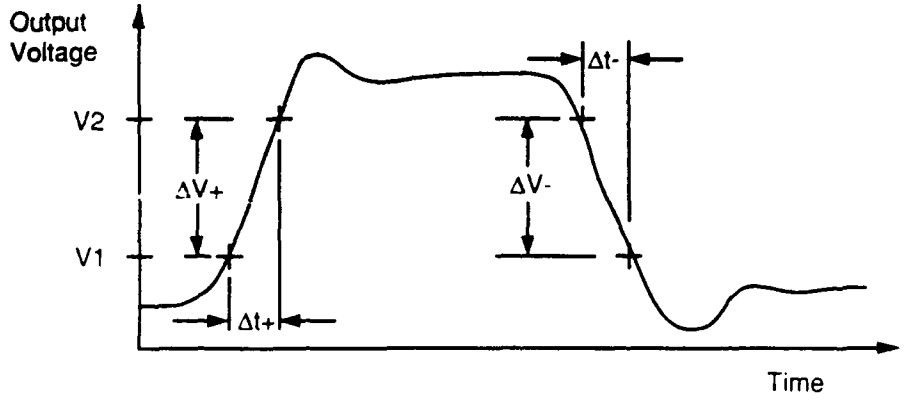
Note: ΔV is allowable error band

Settling Time Waveform
For Positive Switching



Note: ΔV is allowable error band

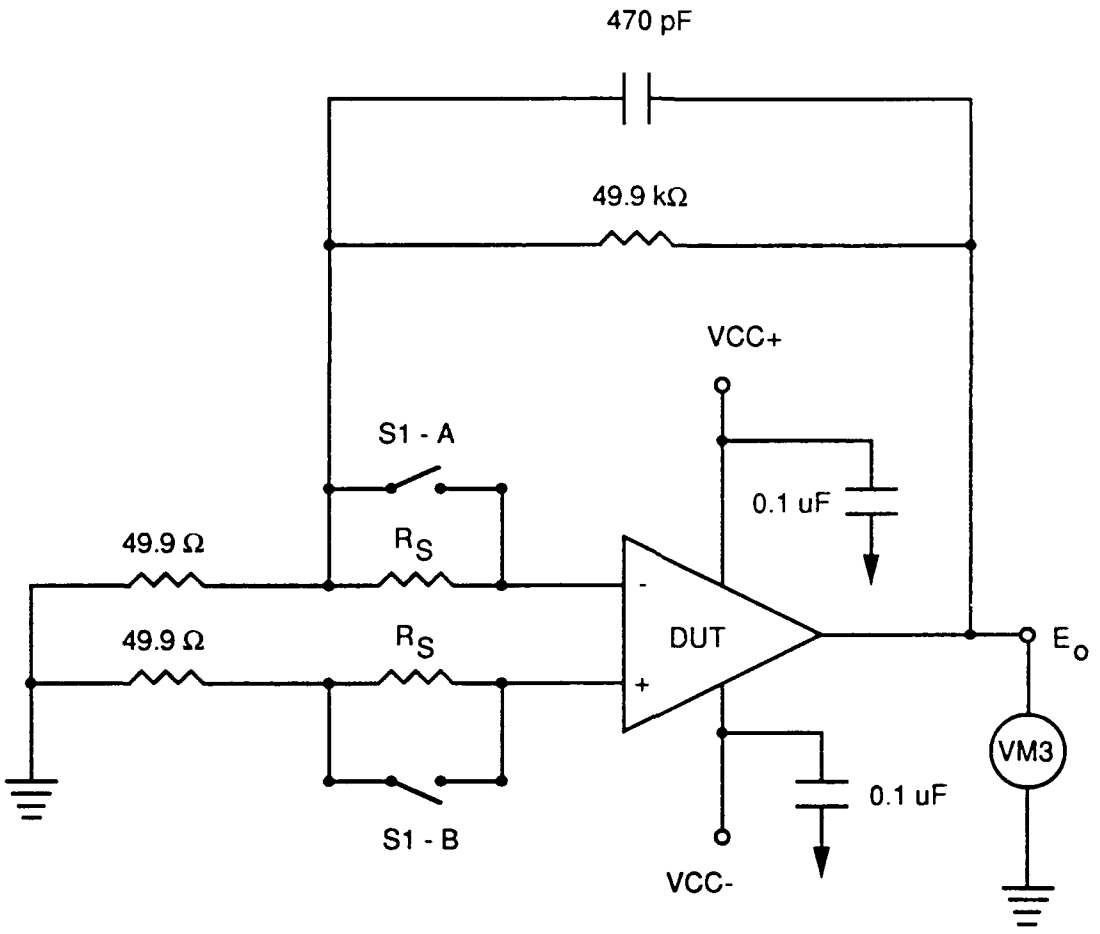
Settling Time Waveform
For Negative Switching



$SR(+) = \Delta V+/\Delta t+$ $SR(-) = \Delta V-/\Delta t-$

Slew Rate Waveform

Figure 6. Dynamic Operational Amplifier Test Waveforms



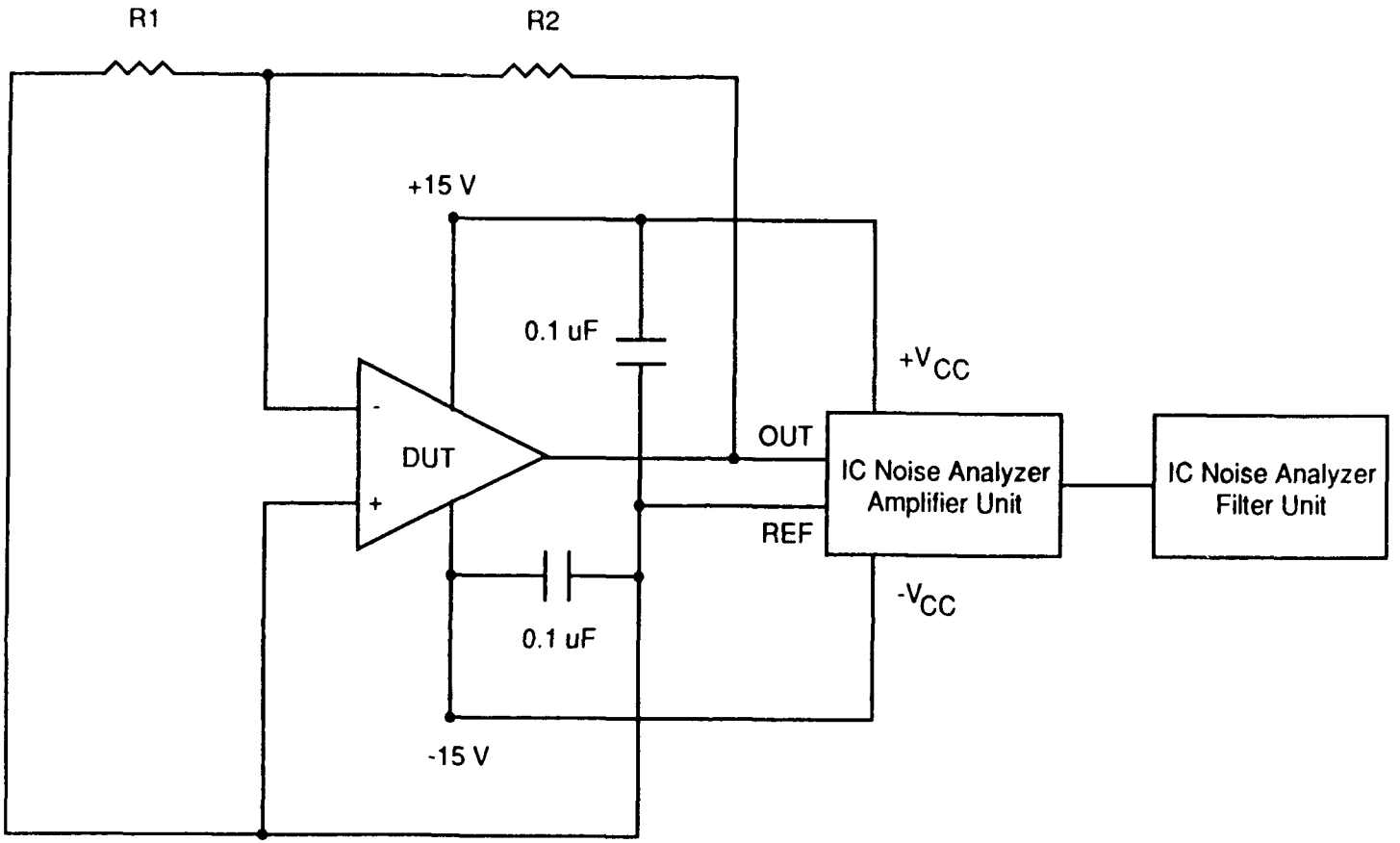
Noise	S1	Measure	Equation	Units
Broadband $N_{I(BB)}$	Closed	E_o	E_o /1000	uV rms
Popcorn $N_{I(PC)}$	Open	E_o	E_o /1000	uV pk

Notes: 1. R_S = 100 kΩ

2. E_o shall be measured with true rms voltmeter with a bandwidth of 10 Hz to 15 kHz (minimum)

3. The 470 pF capacitor and 49.9 kΩ resistor yield a circuit noise bandwidth of 10 kHz

Figure 7. Noise Test Circuit



Notes: 1. Input noise voltage density (En) test: R1 = 50Ω, R2 = 10 kΩ

Input noise current density (In) test: R1 = 105 kΩ, R2 = 2.0 MΩ

2. All resistors have tolerance of +/- 1%, all capacitors have tolerance of +/- 10%.

Figure 8. Noise Density Test Circuit

METHOD 4002

VOLTAGE COMPARATOR PARAMETERS

1.0 PURPOSE. This method establishes the means for measuring input offset voltage, input bias current, common mode input voltage range, common mode rejection ratio, power supply rejection ratio, output leakage current, output short circuit current, output low voltage, power supply current, voltage gain, channel separation and response time for integrated circuit voltage comparators. Equations for calculation of parameters derived from these measurements are included in the method.

1.1 Definitions. The following definitions apply for the purpose of this test method.

1.1.1 Input Offset Voltage (V_{IO}). Input offset voltage is the dc voltage which must be applied between the input terminals to force the quiescent dc output to zero or other specified level.

1.1.2 Input Offset Voltage Drift (DV_{IO}). Input offset voltage drift is the ratio of the change of input offset voltage to the change of circuit temperature. This typically generates a value expressed as microvolts per degree (^{o}C)

$$DV_{IO} = \frac{\Delta V_{IN}}{\Delta T}$$

1.1.3 Input Offset Current (I_{IO}). The input offset current is the algebraic difference between the currents entering into the input terminals of a comparator.

1.1.4 Input Offset Voltage Adjustment Range ($V_{IO}(adj)$). The input offset voltage adjustment ranges are the differences between the offset voltage (V_{IO}) measured with the voltage adjust terminal open circuited and the offset voltage measured with the maximum condition voltage applied to the voltage adjust terminal.

1.1.5 Input Offset Current Drift (DI_{IO}). Input offset current drift is the ratio of the change of input offset current to the change of circuit temperature. This typically generates a value expressed as picoamps per degree (^{o}C).

$$DI_{IO} = \frac{\Delta I_{IO}}{\Delta T}$$

1.1.6 Input Bias Currents ($+I_{IB}, -I_{IB}$). The input bias current is the current that flows in the input lead at a specified input differential voltage. The voltage must be large enough to force the comparator to one of the two stable states.

1.1.7 Common Mode Rejection Ratio (CMRR). The common mode rejection ratio is the ratio of the change in the input common mode voltage to the resulting changes in input offset voltage.

$$CMRR = \frac{\Delta V_{IO}}{\Delta V_{CM}}$$

CMRR is usually expressed in decibels:

$$CMRR = 20\ LOG^{*}\left(\frac{\Delta V_{IO}}{\Delta V_{CM}}\right)$$

1.1.8 Common Mode Input Voltage Range (V_{CMR}). The common mode input voltage range is that range of common mode input voltages which may be applied to the input terminals of the device without decreasing the common mode rejection ratio (CMRR) by more than a specified amount. This parameter is guaranteed by testing CMRR over the specified V_{CMR}.

1.1.9 Power Supply Rejection Ratio (PSRR). The power supply rejection ratio is the ratio of the change in input offset voltage, V_{IO}, to the corresponding change in power supply voltage usually expressed in microvolts per volt. PSRR may be tested either by shifting the voltage of one power supply with all remaining power supply voltages held constant or by shifting both power supply voltages simultaneously. For the first method +PSSR and -PSSR are defined as follows:

$$+PSRR = \frac{\Delta V_{IO}}{\Delta(+V_{CC})} \qquad -V_{CC} = \text{constant}$$

$$-PSRR = \frac{\Delta V_{IO}}{\Delta(-V_{CC})} \qquad +V_{CC} = \text{constant}$$

For the second method, PSRR is defined as:

$$PSRR = \frac{\Delta V_{IO}}{\Delta(V_{CC})}$$

where ΔV_{CC} is obtained by shifting both power supplies, for example, from ± 20 V to ± 5 V.

1.1.10 Output Leakage Current (I_{CEX}). The current measured from the comparator output terminal with the device output in the high state.

1.1.11 Output Low Voltage (V_{OL}). The output voltage in the low state (comparator switched) for a specified sink current.

1.1.12 Output Short Circuit Current (I_{OS}). The maximium positive current that can be delivered by the comparator.

1.1.13 Open Loop Voltage Gain (A_V). The ratio of change in output voltage (over a specified range) to the change in differential input voltage producing it.

1.1.14 Response Time (t_r). The interval between the application of an input step function and the time when the output crosses the logic threshold.

1.1.15 Channel Separation (CS). Channel separation is a measure of interaction between two comparators contained in the same device. It is the ratio of the change in offset voltage of one channel to a change in output voltage in the second channel.

1.1.16 Strobe Pin Function. The strobe pin permits the comparator to be disabled. A low level input to the strobe will cause the output to go to the low state independent of the state of the differential input.

2.0 APPARATUS. The apparatus shall consist of power supplies, current supplies, meters, resistors, and circuit components to implement the circuits shown in figures 1, 3, 4 and 5. Comparator bias power supplies not shown in the figures will also be included in the test circuits.

2.1 DC Voltmeters (VM_1, VM_2). DC voltmeters are required to measure the output voltage of the D/A converter signal from the successive approximation register and the comparator under test in figure 1. In figures 3 and 4 voltmeters measure the output of the nulling amplifier. Voltmeters shall have an input impedance sufficiently high as not to load the circuit under test. Accuracy shall be adequate so that it will have less than ten percent effect on the tolerance specified for the circuit tested. For example if a reading should be 0 $\pm$ 0.1V to be acceptable for the circuit tested, the voltmeter shall be accurate to within $\pm$0.01 V.

2.2 DC Current Meters (CM_1, CM_2). Current meters are required to measure input and output currents from the device. Current meters should be accurate to 0.1% over the range of current to be measured.

2.3 Input Voltage Supplies (VS_1, VS_4). The input voltage supplies shall be capable of forcing positive or negative voltage to the comparator's input terminals. The supplies will have at minimum a resolution of 0.1% and an accuracy of 0.05% over the range of voltages needed for the tests. These voltage supplies must have a programmable mode to simulate an open circuit to effectively remove the supply from the test circuit.

2.4 Output Voltage Supply (VS_3). The output voltage supply must be capable of forcing a specified voltage on the comparator's output. Resolution and accuracy must be equal to that described in section 2.3 for the input voltage supplies. VS_3 must also be capable of being programmed to an open circuit state.

2.5 Reset Current Source (CS_1). To overcome the effects of hysteresis the comparator must be reset between successive approximation trials. This is accomplished with a reset constant current source. The value of the reset current source shall be specified in the procurement document and must be accurate to 0.05%.

2.6 Output Current Supply (CS_2). The output current source is used to place a specified load current on the comparator's output. This current source must be programmable with an accuracy of 0.1%. An open circuit mode must also exist to effectively remove the supply from the test circuit.

2.7 Successive Approximation Loop. This loop consists of the output detector, a successive approximation register (SAR) and a digital-to-analog converter. The detector must be able to compare the output of the comparator and a programmed voltage threshold to determine whether the comparator is in a low or high state. The D/A converter must have the same number of digital inputs as there are bits in the SAR. The full scale voltage of the D/A should be high enough to prevent overranging, and low enough to obtain the proper resolution needed to measure input offset voltage.

2.8 Nulling Amplifier (A1). The nulling amplifier used in figures 3 and 4 amplifies and inverts error voltages at the output of the comparator under test. Recommended type is M38510/135 or superior low offset precision operational amplifier.

2.9 Resistor Networks. The resistors shall be within 1.0% or better of the specified value.

2.10 Bias Power Supplies (+VCC, -VCC). The power supplies shall be capable of supplying maximum required input power to the test circuit. Power supplies must be accurate to 0.1% and capable of being switched to meet the CMRR and PSRR test requirements.

2.11 Pulse Generator (VS_5). The pulse generator used for testing response time in figure 5 shall be capable of driving a 50 ohm impedance to plus or minus the test voltage levels specified in the procurement document at a repetition frequency of 1000 to 10,000 pps.

2.12 Oscilloscope (OSC). The oscilloscope used to measure the response time in figure 5 will be a dual trace type capable of displaying the input and output wave forms of the device under test. The use of a FET probe will be required to minimize errors with devices sensitive to loading.

3.0 PROCEDURE. Input currents and current and voltage at the output of the comparator are measured directly in the circuit of figure 1. Input offset voltage measurements are also made in the test circuit of figure 1 using the successive approximation circuitry to find the input voltage level required for an output change of state. Voltage gain and channel separation are measured with the test circuits shown in figures 3 and 4 which use the nulling amplifier method. Note that with slight modifications, the nulling amplifier circuit shown in figure 3 can be used to measure the majority of the parameters listed in this test procedure. However, use of this method is not recommended for high-speed comparators and these circuits should be measured using the test circuit in figure 1. Dynamic parameters for voltage comparators are measured using the test circuit illustrated in figure 5. The test conditions and measurements are summarized in Table 1.

3.1 Input Currents ($+I_{IB}$, $-I_{IB}$). To measure $+I_{IB}$, switch S_2 is closed to CM_1 providing a path from the non-inverting input of the comparator through CM_1 to ground. Switch S_1 is connected to VS_1. A differential voltage as

specified in the procurement document is applied to the inverting input by VS_1 and $+I_{IB}$ is measured at CM_1. To measure $-I_{IB}$, S_1 is closed to CM_1 and S_2 to VS_1.

3.2 Input Offset Current (I_{IO}). Input offset current can be calculated using the current values measured in section 3.1 by the following equation:

$$I_{IO} = +I_{IB} - (-I_{IB})$$

3.3 Input Offset Current Drift (DI_{IO}). Measurement of I_{IO1} is made at temperature T_1 and I_{IO2} at temperature T_2 following sections 3.1 and 3.2. Then:

$$DI_{IO} = \frac{I_{IO2} - I_{IO1}}{T_2 - T_1}$$

3.4 Output Leakage Current (I_{CEX}). The output leakage current test is applicable to comparators with open collector outputs. Switch S1 is closed to CS_1 and S_2 to ground via CM_1. All other switches are open. Current output from CS_1 is programmed to result in a voltage drop across R_3 providing the differential voltage at the inputs required to place the output of the comparator in the output high state. Typically the differential voltage drop will be less than 0.5 volts. If $R_3 = 100\Omega$ then +2 mA sourced by CS_1 will provide 200 mV differential voltage at the inputs of the comparator which will be sufficient for most devices. Output voltage supply, VS_3, is then set to a level specified by the procurement document for measurement of output leakage current. I_{CEX} is measured using CM_2.

3.5 Output Low Voltage (V_{OL}). The output low voltage is measured with the comparator output set to the low state specified in the procurement document. Switch S_1 is closed to CS_1 and S_2 to ground through CM_1. S_6 is closed to connect resistor R_6, the load resistor. R_6 will be a resistance specified in the procurement document. All other switches are open. Output voltage supply, VS_3, is disconnected from the output. CS_1 is programmed to supply a differential voltage at the inputs sufficient to put the output transistor of the comparator in the output low state. The test load current specified in the procurement document is applied from CS_2 and V_{OL} measured using VM_2.

3.6 Output Short Circuit Current (I_{OS}). Output short circuit current is measured with the comparator output set to the high state. Switch S_1 is closed to CS_1 and S_2 to ground through CM_1. S_6 is closed to connect resistor R_6, the load resistor. All other switches are open. Output voltage supply, VS_3 is programmed to the test voltage specified in the procurement document. CS_1 is programmed to supply a differential voltage at the inputs sufficient to put the output transistor of the comparator in the output high state. I_{OS} is measured at CM_2. The short circuit condition should be limited to 10 ms duration unless otherwise specified in the procurement document.

3.7 Input Offset Voltage (V_{IO}). Input offset voltage is measured in the circuit of figure 1 using the SAR circuitry. Switch S_1 is closed to the summing node for V_A, V_{CORR} and CS_1. The hysteresis loop is completed by closing switch S_2 to resistor R_4 and closing S_3. S_4 and S_5 are closed to place the SAR circuitry in the feedback loop and S_6 is closed to insert the load resistor. The procedure uses the SAR to locate the comparator input transition voltage at which the output changes from V_O(low) to V_O(high).

Hysteresis is used assure fast switching and is obtained by feeding back a fraction of the output voltage to the non-inverting input via the feedback network R_5, R_4. This fed back portion of the output voltage causes a shift in the transition point and must be compensated for by adding an equal voltage at the inverting input. This is accomplished by supplying V_{CORR} from VS_1. Current supply CS_1 is used to reset the comparator output level to V_O(low) between adjustments to V_A by the successive approximation circuitry. This assures that the transition will always be approached from the same direction. The magnitude of the reset current should be such as to produce a voltage at the negative input sufficient to cause reset. For typical comparators this will be of the less than 0.5 volts. A current of 2 mA will add 200 mV to the voltage at the input summing point of the comparator.

The adjust voltage, V_A, is divided by the resistor R_2, R_4 and, therefore, the full scale voltage of the D/A converter component of the SAR circuitry should be set equal to R_2/R_1 times V_{IO}(maximium) specified for the comparator in test or a value slightly higher. For R_2= 9.9 kΩ and R_4 = 100Ω, V_{CORR} = 100 times V_{IO}(max).

The procedure for measurement of V_{IO} begins with a measurement of V_O(low). Sufficient current is supplied from CS_1 to place the comparator output in the low state and V_O(low) is measured at VM_2. The value of V_{CORR} is then calculated and programmed to power supply VS_1.

V_{CORR} is calculated as follows:

$$V_{CORR} = \frac{R_4}{R_5} * \frac{R_1 + R_3}{R_3} * V_O(\text{low})$$

where V_O(low) is the output low voltage under the test conditions. For example, if the feedback ratio (R_4/R_5) is 1/1000 and the divider ratio for V_{CORR}, ($R_3/(R_1+R_3)$), is 1/100, then $V_{CORR} = 10*V_O(\text{low})$.

A graphic example of the successive approximation process is shown in figure 2. The process begins with an initial trial value of zero volts for the adjust voltage V_A. The output detector determines the state of the comparator. If the output state is high, the successive approximation register and D/A converter will supply a more positive voltage, if low, a more negative voltage. The successive approximation register continues to generate adjustments of decreasing magnitude until V_A converges on a final value. The current source CS_1 is switched on in the first half of each clock cycle to reset the converter to the low level. The final adjust voltage V_A is measured using VM_1 and V_{IO} calculated as follows:

$$V_{IO} = \frac{R_3}{R_2 + R_3} * V_A \qquad \text{volts}$$

3.8 Input Offset Voltage Drift (DV_{IO}). Measurements of input offset voltage, V_{IO1} and V_{IO2} are made at temperature T_1 and T_2 following the method of section 3.7. DV_{IO} is calculated as:

$$DV_{IO} = \frac{V_{IO2} - V_{IO1}}{T_2 - T_1}$$

3.9 Input Offset Voltage Adjustment Range ($V_{IO}(adj)$). Offset voltage adjustment range is determined from measurements of V_{IO} at each extreme of adjustment. The configuration of the adjust network in each case will be specified in the procurement document. Switch settings are as in section 3.7 except that S_7 is closed. Two values are measured. $V_{IO}(+)$ is measured with the maximum positive condition applied to the adjust terminal, and $V_{IO}(-)$ is measured with the maximum negative condition applied. These two values are then compared with the value of V_{IO} measured with S_7 open to obtain the adjustment range:

$$V_{IO}(adj+) = V_{IO} - V_{IO}(+); \qquad V_{IO}(adj-) = V_{IO} - V_{IO}(-)$$

3.10 Common Mode Rejection Ratio (CMRR). The circuit of figure 1 is configured as in section 3.7 to measure input offset voltage. A common mode voltage is applied to the inputs of the comparators by shifting both VCC power supplies an equal amount in the same direction, first more positive then more negative. For example, if nominal VCC is $\pm$15 volts, then pairs of power supply levels may be +5V, -25 and +25V, -5V for a common mode shift of 20 volts. The input offset voltage is measured for each power supply condition. CMRR is calculated as:

$$CMRR = \frac{\Delta V_{CC}}{\Delta V_{IO}} \qquad \text{Volts/Volt}$$

where: CMRR = Common mode rejection ratio
ΔV_{IO} = Change in input offset voltage
ΔV_{CC} = Change in power supply voltages

The units are normally adjusted to millivolts per volt or microvolts per volt. Common mode rejection ratio can also be expressed in decibels:

$$CMRR = 20*LOG \left(\frac{\Delta V_{CC}}{\Delta V_{IO}} \right) \qquad \text{decibels}$$

3.11 Common Mode Input Voltage Range. This test confirms that the common mode input voltage specification is met over a specified range of common mode voltages. The test is performed concurrently with CMRR by having the maximum and minimum common mode voltages applied to the input terminals of the comparator during the test described in section 3.10.

3.12 Power Supply Rejection Ratio (PSRR). Power supply rejection ratio may be obtained by determining the change in offset voltage for a change in one power supply voltage with all other power supply voltages held constant.

Alternatively, more than one supply may be varied at the same time. The variation will be as specified in the procurement document. Input offset voltage is measured as described in section 3.7.

$$PSRR = \frac{\Delta V_{IO}}{\Delta V_{CC}}$$

where: ΔV_{IO} = Change in offset voltage
ΔV_{CC} = Change in power supply voltage

3.13 Power Supply Current (ICC). Power supply current shall be measured for all device bias supplies using method 3005.1 of MIL-STD-883C.

3.14 Voltage Gain (A_V). When required by the procurement document, voltage gain is measured using the circuit shown in figure 3. The circuit should be constructed with good wiring practices and include bypass capacitors to reduce the possibility of oscillation. The stabilizing capacitors shown in the circuit may not be appropriate or may not be adequate for the specific comparator tested. Proper stabilization methods for the device tested should be obtained from the procurement document. Load resistor R_L will also be specified in the procurement document. The procurement document may specify a level of oscillation at which the device is considered to fail the test. This level should be monitored at the oscillation detector.

The comparator output voltage levels, V_{O1} and V_{O2}, between which gain is to be measured will be specified in the procurement document. These voltages are applied successively to the inverting input of the nulling amplifier using VS_1. For each level the circuit is allowed to settle, and E_1 and E_2 are measured using VM_1.

$$A_V = \frac{V_{O2} - V_{O1}}{\Delta V_{IN}} \quad \text{Volts/Volt}$$

where $\Delta V_{IN} = (E_2 - E_1)*(R_1/R_2)$

3.15 Channel Separation (CS). Channel separation for dual and quad voltage comparators is tested in the circuit of figure 4. CS is tested for each comparator with respect to all other comparators. Thus two tests are performed for a dual comparator and 12 for a quad comparator. The test circuit of figure 4 is applicable to both dual and quad comparators. The connection shown is for measurement of comparator B output sensitivity with respect to a signal applied to the input of comparator A. Comparators C and D, if present, are connected as shown. The comparator supply voltages, $\pm$VCC, and the nominal comparator output voltage, V_O, should be as specified in the procurement document. Input voltages are applied to the switched comparator to drive the output successively to the high and low states, for example +1 and -1 volt. The nulling amplifier outputs, E_1 and E_2, are measured for each condition.

The high and low output voltages of the switched comparator can be taken as +VCC and -VCC for the purposes of this measurement. Then the voltage change at the output of comparator A is:

$$\Delta V_O(A) = (+VCC) + (-VCC)$$

The change of input voltage at the input of comparator B is found by dividing the measured change by the loop gain:

$$\Delta V_{IN}(B) = \frac{E_1 - E_2}{1000}$$

Channel separation is then found from:

$$CS = 20*LOG \left(\frac{\Delta V_O(A)}{\Delta V_{IN}} \right) \qquad \text{decibels}$$

3.16 Strobe Function Test. This test is performed in the circuit of figure 1. The strobe pin of the comparator is set to the limit level for the enabled condition and the required differential voltages are applied to the comparator inputs to switch the output between states. The comparator output state is monitored with the output voltmeter, VM_2, and should show proper switching action. The strobe pin is then set to the limit level for the disabled condition and the same differential input levels are applied to the comparator while the output is observed at VM_1. The output should not exhibit switching action.

3.17 Response time (t_r). Response time is measured in the circuit of figure 5. Input and output waveforms are displayed on the oscilloscope and t_r obtained as indicated.

3.18 Optional Test Procedures Using the Nulling Amplifier Test Method. As previously mentioned, several comparator parameters can be measured using the nulling amplifier test circuit shown in figure 3. These parameters are briefly listed in this section and reference method 4001 which describes the test procedures used for operational amplifiers.

Input Bias Currents ($+I_{IB}$, $-I_{IB}$) and Input Offset Current (I_{IO}): Use the procedure outlined in method 4001. For these tests the circuit shown in figure 3 will have to modified to include bypass switches and large MΩ resistors in each of the differential inputs of the comparator. As also mentioned in method 4001, comparators with low leakage currents can use the optional integrated capacitor test method to obtain these values.

Input Offset Voltage (V_{IO}) and Adjustment Range ($V_{IO}(adj)$): Use the procedure outlined in method 4001. Note that several types of comparators, particularly high-speed comparators, are not amenable to being tested in this manner. For these device types, the procedures outlined in this test method are recommended.

Common Mode Rejection Ratio (CMRR), Common Mode Voltage Range (VCM), Power Supply Rejection Ratio (PSRR): Use the procedures outlined in method 4001. Again, measurement of V_{IO} may be difficult for some part types using this method.

4.0 SUMMARY. The following details shall be specified in the applicable procurement do cument.

a. +VCC and -VCC for each test
b. Input voltages to be applied by VS_1 for the I_{CEX}, V_{OL}, and I_{OS} tests
c. Voltage for V_{CORR}
d. Threshold voltage for the output detector
e. Load current to use for V_{OL} test
f. Forced output voltage for I_{CEX} test
g. ΔVCC values for PSRR and CMRR tests
i. Resistor values for each device type
j. Limit values for each parameter tested
k. Condition and component values for response time
l. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient

PARAMETER	SWITCHES					SOURCES				MEASUREMENT		EQUATIONS	UNITS	NOTES
	S1	S2	S3 S4 S5	S6	S7	VS_1	VS_3	CS_1	CS_2	METER	VALUE			
$+I_{IB}$	P2	P6	OPEN	OP	OP	V_{IN-}	OPEN	OPEN	OPEN	CM_1	I_1	$+I_{IB} = I_1$	AMPS	
$-I_{IB}$	P3	P5	OPEN	OP	OP	V_{IN+}	OPEN	OPEN	OPEN	CM_1	I_2	$-I_{IB} = I_2$	AMPS	
I_{IO}	--	--	----	--	--	----	----	----	----	---	---	$I_{IO} = I_1 - I_2$	AMPS	
I_{CEX}	P1	P6	OPEN	OP	OP	OPEN	V_{OUT}	I_{IN}	OPEN	CM_2	I_3	$I_{CEX} = I_3$	AMPS	NOTE 2
V_{OL}	P1	P6	OPEN	CL	OP	OPEN	OPEN	I_{IN}	I_L	VM_2	E_1	$V_{OL} = E_1$	VOLTS	NOTE 2
I_{OS}	P1	P6	OPEN	CL	OP	OPEN	V_{OUT}	I_{IN}	OPEN	CM_2	I_4	$I_{OS} = I_4$	AMPS	NOTE 2
V_{IO}	P1	P4	CLOSED	CL	OP	V_X	OPEN	I_X	OPEN	VM_1	E_2	$V_{IO} = \frac{R_3}{R_2 + R_3} * E_2$	AMPS	NOTE 3
$V_{IO}(adj)$	P1 P1	P4 P4	CLOSED CLOSED	CL CL	CL CL	V_X V_X	OPEN OPEN	I_X I_X	OPEN OPEN	VM_1 VM_1	E_3 E_4	$V_{IO}(adj+) = E_2 - E_3$ $V_{IO}(adj-) = E_2 - E_4$	VOLTS VOLTS	NOTE 3
CMRR	P1 P1	P4 P4	CLOSED CLOSED	CL CL	OP OP	V_X V_X	OPEN OPEN	I_X I_X	OPEN OPEN	VM_1 VM_1	E_5 E_6	$CMRR = 20 * \left(\frac{\Delta V_{CC}}{E_6 - E_5} \right)$	db	NOTE 3 NOTE 4
PSRR	P1 P1	P4 P4	CLOSED CLOSED	CL CL	OP OP	V_X V_X	OPEN OPEN	I_X I_X	OPEN OPEN	VM_1 VM_1	E_7 E_8	$PSRR = \frac{E_8 - E_7}{\Delta V_{CC}}$	NONE	NOTE 3 NOTE 5

Notes:
1. OP signifies switch OPEN, CL signifies switch CLOSED
2. I_{IN} is the current required to create a differential voltage sufficient to set the comparator output to the required state
3. V_X and I_X are set depending on values measured while using the SAR procedure described in section 3.7
4. E_5 measured with power supplies at nominal level, E_6 measured after both power supplies have been set to the adjusted level
5. E_7 measured with power supply at nominal level, E_8 measured with power supply at adjusted level

Table 1. Equations For Comparator Tests

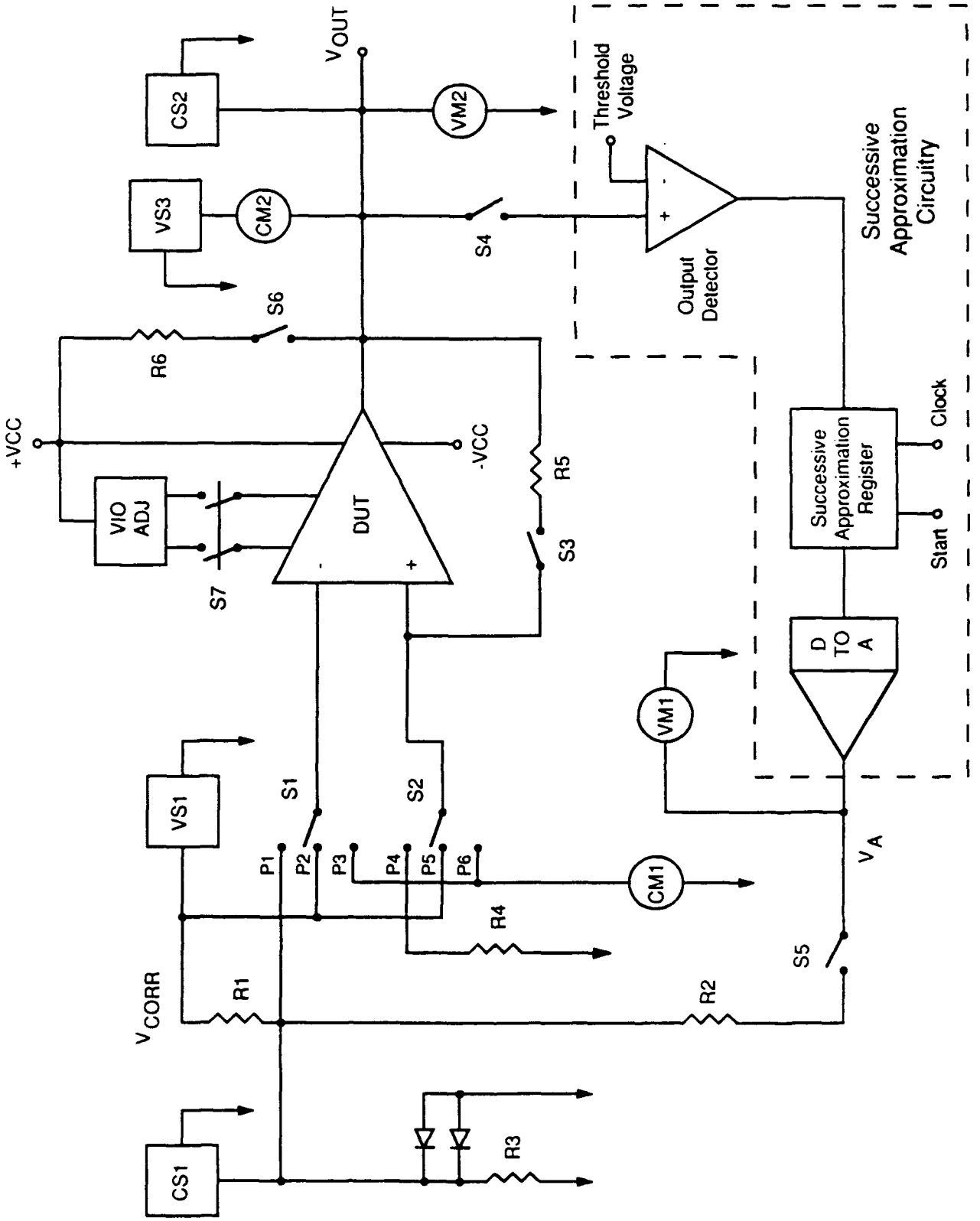
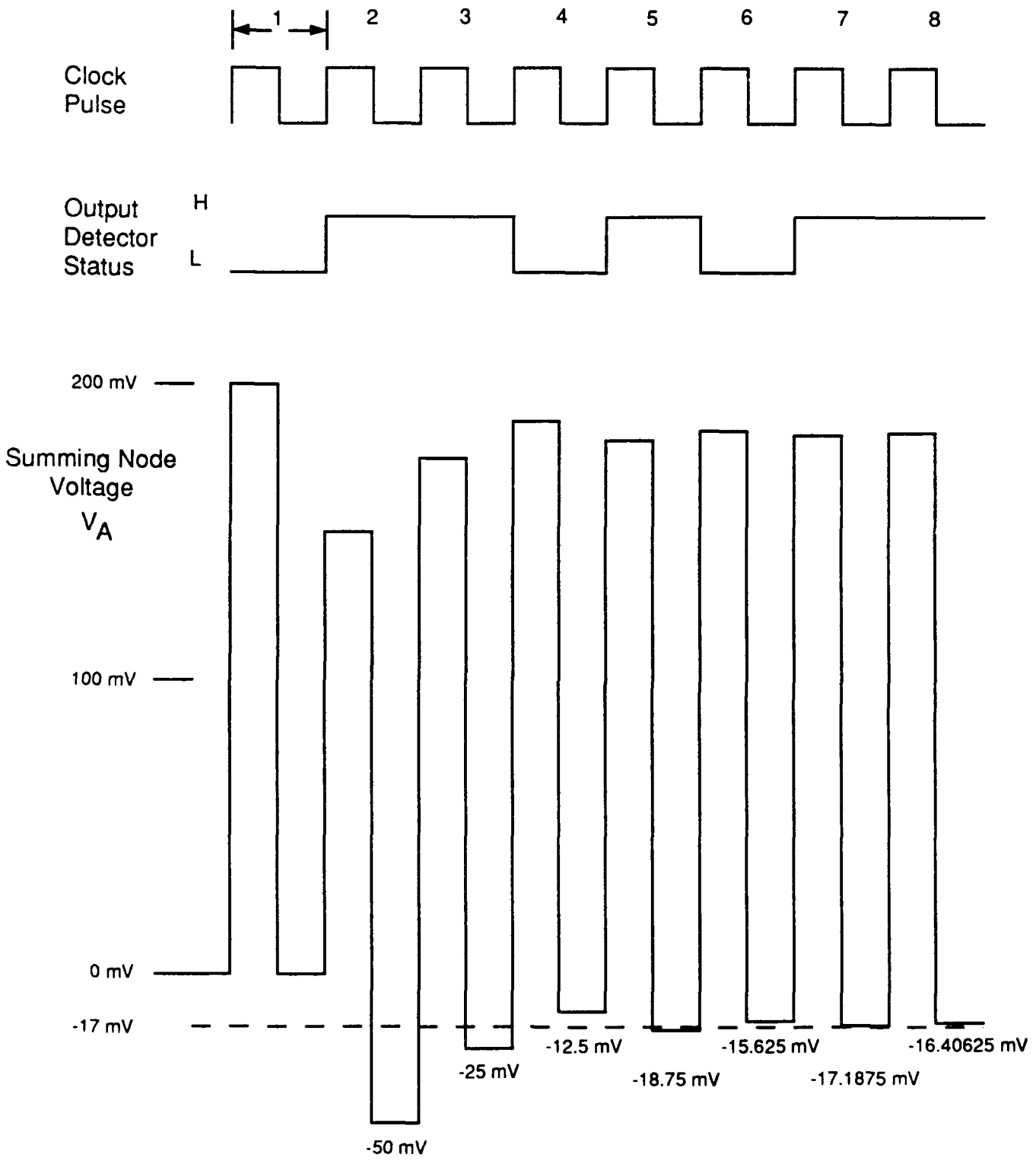
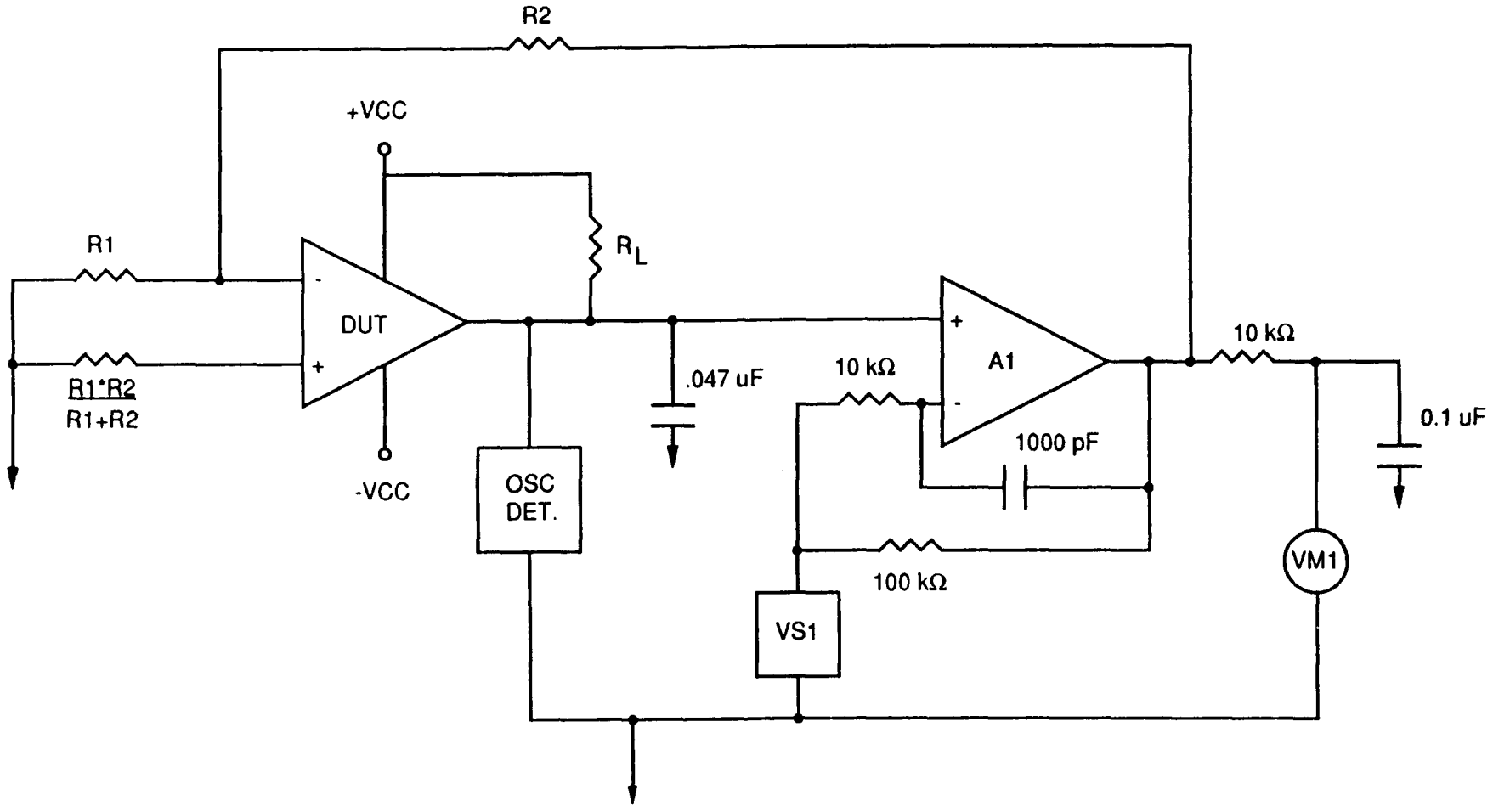


Figure 1. Comparator Test Circuit



Notes: 1. Assumes 8-Bit D/A Converter and SAR used
2. D/A Converter full scale voltage = 100 mV
3. Actual offset is -17 mV

Figure 2. Successive Approximation Process Used to Find Offset of -17 mV

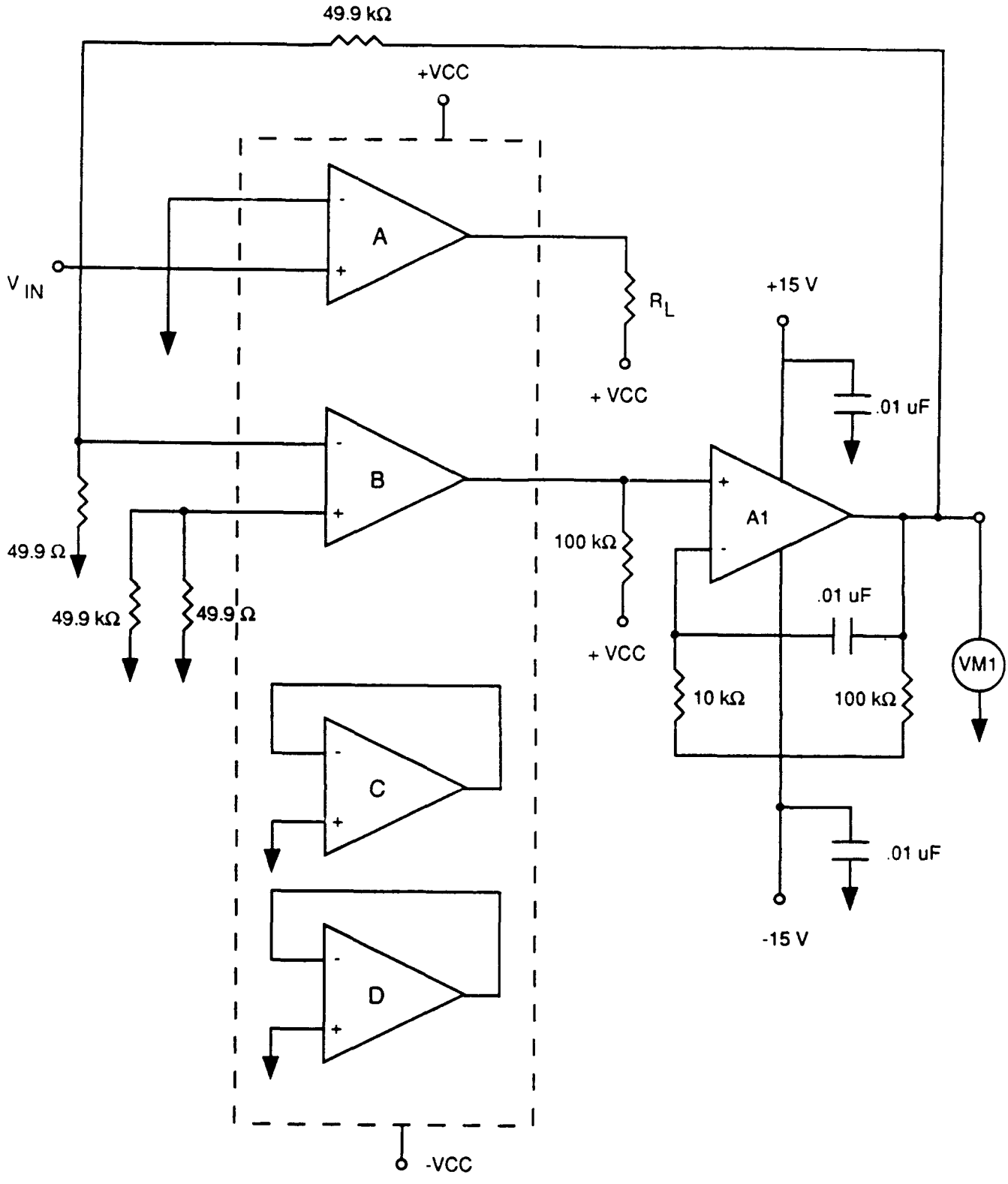


Notes: 1. R1 = 49.9Ω, R2 = 49.9 kΩ unless otherwise specified in the procurement document

2. R1 and R2 must have a tolerance within ± 0.1%

3. Stabilization capacitors shown may not be suitable for all devices

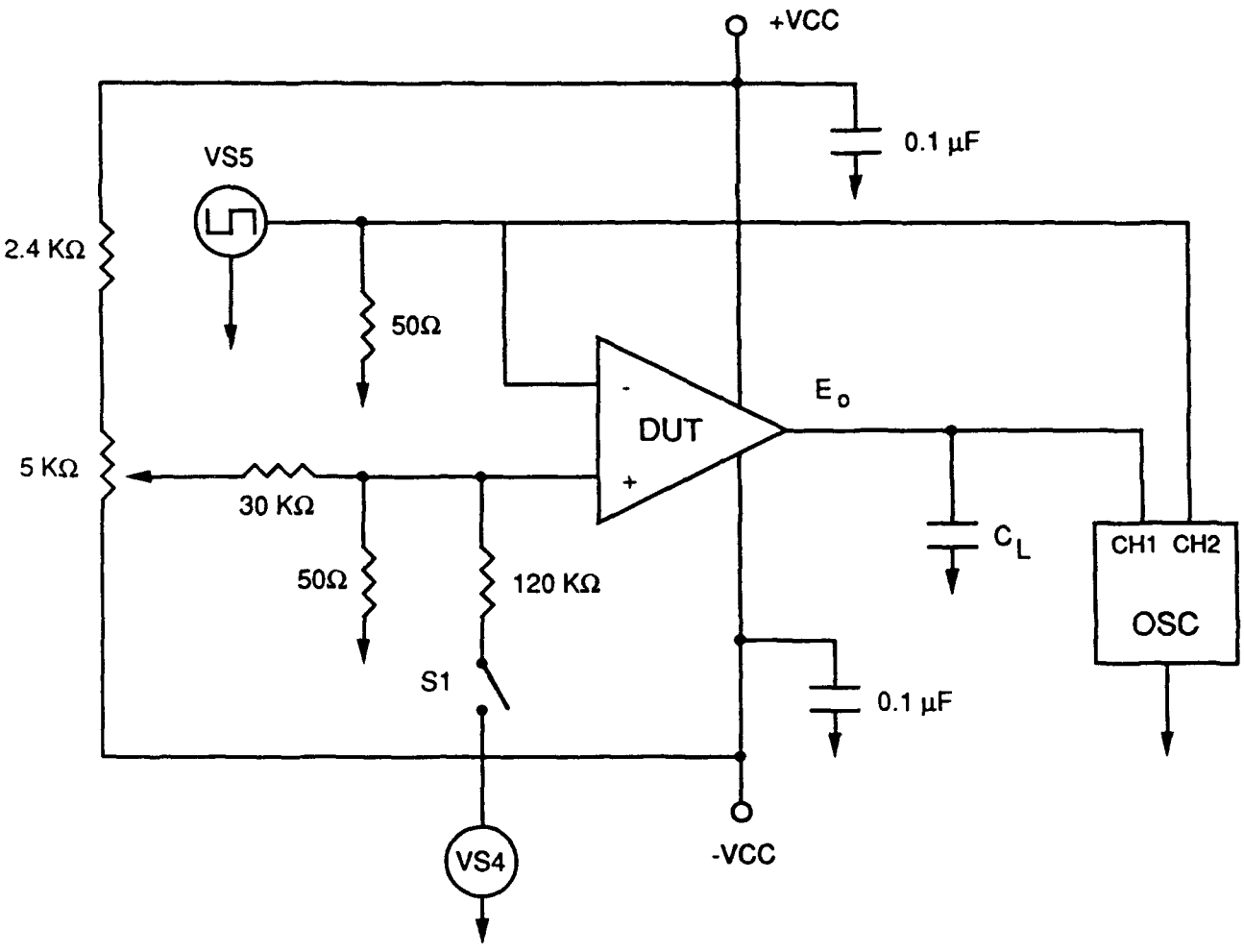
Figure 3. Voltage Gain Test Circuit

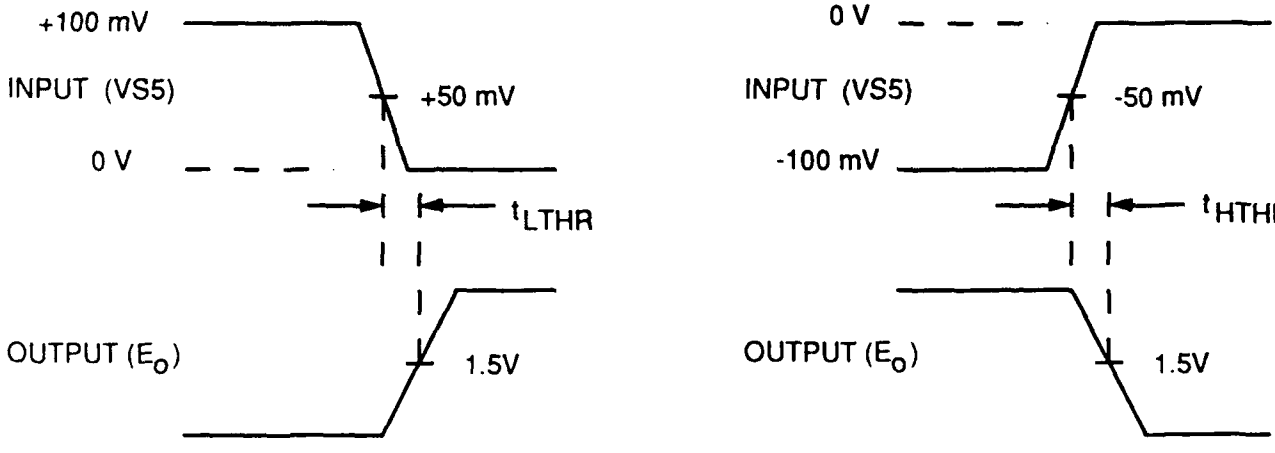


Notes: 1. All resistors +/- 0.1% tolerance, all capacitors +/- 10% tolerance

2. The nulling amplifier shall be MIL-M-38510/135 or similar. Saturation of the amplifier is not allowed

Figure 4. Channel Separation Test Circuit





VS4 = +12 V
S1 = Closed

VS4 = -12 V
S1 = Closed

Figure 5. Response Time Circuit and Waveforms

METHOD 4003

VOLTAGE REFERENCE PARAMETERS

1.0 PURPOSE. This method establishes the means for measuring output voltage, load regulation, line regulation, quiescent current, output short circuit current, turn-on settling time, noise output, and voltage output temperature coefficient of monolithic silicon, fixed and pin programmable linear voltage references.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Pin Programmable. Pin programmable refers to a voltage reference with multiple high-precision output voltage levels. Specific voltages are obtained by connecting combinations of device pins to the reference output pin.

1.1.2 Voltage Output Pins. The voltage output pins are the device pins across which the stabilized precision voltage of the reference can be measured. For pin programmable voltage references, the voltage output pin may actually be a node consisting of two or more device pins.

1.1.3 Output Voltage (V_{OUT}). The stable voltage across the voltage output pins of the voltage reference.

1.1.4 Supply Voltage (V_{IN}). The voltage supplied at the input of the voltage reference.

1.1.5 Input Voltage Range. The range of input supply voltage over which the reference will operate.

1.1.6 Load Regulation (VR_{LOAD}). The change in output voltage for a specified change in the load current under a constant input voltage.

1.1.7 Line Regulation (VR_{LINE}). The change in output voltage for a specified change in input voltage under a constant load current.

1.1.8 Output Short Circuit Current (I_{OS}). The current from the voltage output pin of the voltage reference when the voltage across the output pins is at zero volts.

1.1.9 Quiescent Current (I_Q). The power supply current required to operate the voltage reference under a no-load condition.

1.1.10 Turn-on Settling Time (t_{PS}). The time required for the voltage reference output to settle within a specified error band from a cold start.

1.1.11 Noise Output (N_O). The noise output from the voltage reference for a specified voltage and bandwidth. Noise is measured for two pass bands. Low frequency noise is measured at frequencies appropriate for 1/f noise. This noise voltage is measured as peak-to-peak voltage for the

specified bandwidth. High frequency noise is measured with a pass band suitable for white noise measurement. This noise voltage is measured as rms voltage for the specified bandwidth.

1.1.12 Output Voltage Temperature Coefficient (DV_{OUT}/DT). The percentage change in voltage reference output voltage per degree centigrade.

2.0 APPARATUS. The apparatus shall consist of programmable voltage sources, a programmable current source, a switching network, voltmeters, current meters, and capacitors to implement the circuit of figure 1. An oscilloscope and suitable buffering circuitry are required for measuring turn-on settling time and low frequency noise.

2.1 DC Voltmeter (VM1). The voltmeter used to measure the output voltage of the reference under test should be accurate to 0.01% of the nominal output voltage. The response time of the voltmeter to a change in voltage will be equal to or better than 0.1 times the minimum time specified for the voltage reference to respond to changes in line voltage and load current. For example, if the reference is specified to respond within 1 ms the voltmeter should be capable of responding within 0.1 ms. The voltmeter will be programmable to make a measurement at a specified interval after the application of a strobe coincident with programmed changes in line voltage or load current.

2.2 AC Voltmeter (VM2). The AC rms voltmeter is used to measure the high frequency (white) noise output from the voltage reference. The voltmeter shall have a bandwidth of 50 HZ to 100 KHZ.

2.3 Noise Amplifier. The noise amplifier shall have two channels, one for low freqency noise measurements, the other for mid band high frequency (white) noise measurements. The low frequency channel shall have a bandwidth of 0.1 HZ to 10 KHZ and sufficient gain to provide displayed signals on an oscilloscope after amplification with a pre-amplifier. The high frequency channel shall have a gain bandwidth product greater than 10 MHZ.

2.4 DC Current Meters (CM1, CM2). Programmable current meters are required to measure output short circuit current and quiescent current. The current meters should be accurate to 0.1% over the range of current to be measured. Additionally, the current meter used to measure the short circuit output current must be programmable to make a measurement at a specified time following the application of the short circuit voltage condition at the voltage output pin.

2.5 Programmable Input Voltage Supply (VS_1). The programmable input voltage supply will be capable of forcing positive or negative voltage with sufficient current over the range specified for the reference under test. The input supply will be digitally programmable to a resolution of 0.1% and with an accuracy of 0.05%. It must also be capable of providing a voltage pulse of duration specified in the voltage reference procurement document. The input voltage supply will be provided with separate sense and power inputs.

2.6 Programmable Output Voltage Supply (VS_2). The function of the output voltage supply is to simulate a transient short circuit at the

voltage output pin of the reference under test. This supply will be capable of providing a voltage pulse. The supply must also be able to administer this pulse within a time interval specified in the procurement document to prevent thermal damage. A programmable open mode must also exist, which will enable the equivalent of switching the output voltage supply out of the reference load path. The output voltage source will be programmable to an accuracy of 0.1% of the nominal reference output voltage and capable of sourcing or sinking current greater than the maximum short circuit current specified for the reference in test. Separate sense and power inputs/outputs will be provided.

2.7 Programmable Output Current Supply (CS). The programmable output current supply will be capable of sourcing or sinking current to an accuracy of 0.1% over the range of output currents specified for the reference in test. The output current supply will be programmable to generate a current pulse of amplitude and width specified for measurement of load regulation of the device. It must also have the ability to be programmed to an open circuit (no current) condition.

2.8 Switching Network. This network is only required for pin programmable voltage references. It will consist of the necessary relays or switches to allow each programming pin to be connected the voltage output pin. The network should be devised such that all combinations of pin connections can be made. An example of such a network is shown in figure 1.

2.9 Oscilloscope and Buffer Circuitry. These items are required for the turn-on settling time measurement and noise output measurement. The oscilloscope input impedance will be at least 1 megaohm and the bandwidth must be at least 100 times that of the worst case voltage pulse to be measured. The oscilloscope must also have the capability to be triggered externally by the power supply input. The buffer circuitry should be designed such that the turn-on voltage pulse by the input supply will not damage the oscilloscope. Noise output measurement requires a pre-amp of the DC voltage comparator type for peak-to-peak voltage measurements.

2.10 3-Way Switch (S1). This switch is used to connect additional test circuitry to the output of the voltage reference under test. The normal position of the switch, position 1, removes all additional equipment from the circuit. Position 2 adds the oscilloscope used for the turn-on settling time test. Position 3 adds the oscilloscope, noise amplifier, and AC voltmeter for both of the noise tests.

3.0 PROCEDURE. Figure 1 shows the generic test configuration for fixed and pin programmable voltage references. Procedures for specific tests are described below and summarized in Table 1.

3.1 Output Voltage (V_{OUT}). The output voltage of the reference in test is measured across the voltage output pin with voltmeter VM1. For this test and all others, switch S1 is placed at position 1 unless otherwise specified. The input voltage supply (VS_1) is set to the specified input voltage, V_{IN}, the load current supply (CS) is set to the specified load current, I_L, and the short circuit current voltage supply (VS_2) is set to the open condition. For pin programmable voltage references, the switching

network is configured such that the proper output level is being tested for. V_{OUT} is then measured and the deviation from the ideal value is calculated. For pin programmable references this measurement will be repeated for every combination listed in the procurement document.

3.2 Load Regulation (VR_{LOAD}). Load regulation is obtained from two measurements of V_{OUT} at two different values of load current specified in the procurement specification. The output voltage, E_1, is first measured at an initial load current, I_{L1}. The load current supply is then switched to a value of I_{L2} and E_2 is measured at a specified time after the current transition takes place as shown in the waveform diagram of figure 2. Load regulation is calculated as:

$$VR_{LOAD} = E_2 - E_1$$

Note that multiple measurements of VR_{LOAD} may be required for pin programmable references.

3.3 Line Regulation (VR_{LINE}). Line regulation is obtained from two measurements of V_{OUT} at two different values of input line voltage, V_{IN}, as specified in the procurement specification. E_3 is measured at an initial line voltage V_{IN1}, provided by the input voltage supply (VS_1). VS_1 is then pulsed to a value V_{IN2} and E_4 is measured at a specified time after the input voltage transition to V_{IN2} takes place as shown in figure 2. The output conditions set by VS_2 and CS remain constant between the two measurements. Line regulation is calculated as:

$$VR_{LINE} = E_4 - E_3$$

3.4 Short Circuit Output Current (I_{OS}). The short circuit current is measured by current meter CM2 while the voltage output pin of the reference is pulsed to ground reference level by the output voltage supply, VS_2. The reference input/output conditions are set as specified in the procurement document and the current supply (CS) set to the open condition which effectively removes it from the circuit. The pulse by VS_2 is then applied to the voltage output pin and the measurement made at a time, t_{OSS}, after the initiation of the pulse (see the waveforms of figure 2). The duration of the pulse and t_{OSS} will also be specified in the procurement document.

3.5 Quiescent Current (I_Q). The quiescent current is measured by current meter CM1 while the reference is in an unloaded condition. The input voltage supply (VS_1) is set to a level specified in the procurement document, and both VS_2 and CS are set to the open circuit condition to simulate an unloaded condition. For pin programmable references the switching network is configured to place the output voltage at a nominal level. Quiescent current is then measured by CM1.

3.6 Turn-on Settling Time (t_{ps}). This test makes use of the oscilloscope and buffer circuitry shown in the test circuit of figure 1. This equipment is switched in by placing S1 at position 2 while performing the test. Turn-on settling time is also measured with the reference in an unloaded condition which is achieved by setting both VS_2 and CS to the open circuit condition. The switching network should be configured to place the output voltage at a nominal level specified in the procurement document.

The input power supply (VS_1) is connected to channel 2 of the oscilloscope through the buffer circuitry and is initially in the off-state. When turned on, the oscilloscope will be able to capture the response of the voltage reference in test. Turn-on settling time is measured from the time VS_1 is turned on, to the time when the output voltage of the reference is within a predefined limit of nominal V_{OUT} (see figure 2). The value of this error band limit is specified in the procurement document.

3.7 Noise Voltage (Low Frequency) (N_O). This test makes use of the oscilloscope and noise amplifier shown in figure 1. Switch S1 is set to position 3 which will switch in both pieces of equipment. The output signal is connected to the low frequency channel of the noise amplifier which must have a pass band of 0.1 HZ to 10 HZ for this measurement. The output from the noise amplifier is then amplified with a DC comparator type pre-amplifier before being input to the oscilloscope. With the oscilloscope time base set to display frequencies down to 0.1HZ, the peak-to-peak voltage shall be measured.

3.8 Noise Voltage (High Frequency) (N_O). This test makes use of the noise amplifier and AC voltmeter shown in figure 1. Switch S1 is again set to position 3 to route the output signal of the voltage reference to the high frequency channel of the noise amplifier. This channel must have a pass band of 10 HZ to 100 KHZ for high frequency (white) noise measurements. The noise voltage is measured with the AC voltmeter (VM2) for a specified DC output voltage.

3.9 Output Voltage Temperature Coefficient (DV_{OUT}/DT). To determine this coefficient, the output voltage of the reference under test is measured at two specified temperatures. All test conditions except temperature should be identical when making these measurements. The output voltage temperature coefficient is then calculated as:

$$DV_{OUT}/DT = \frac{\Delta V_{OUT}}{\Delta T}$$

where ΔV_{OUT} is the change in output voltage for the change in temperature ΔT.

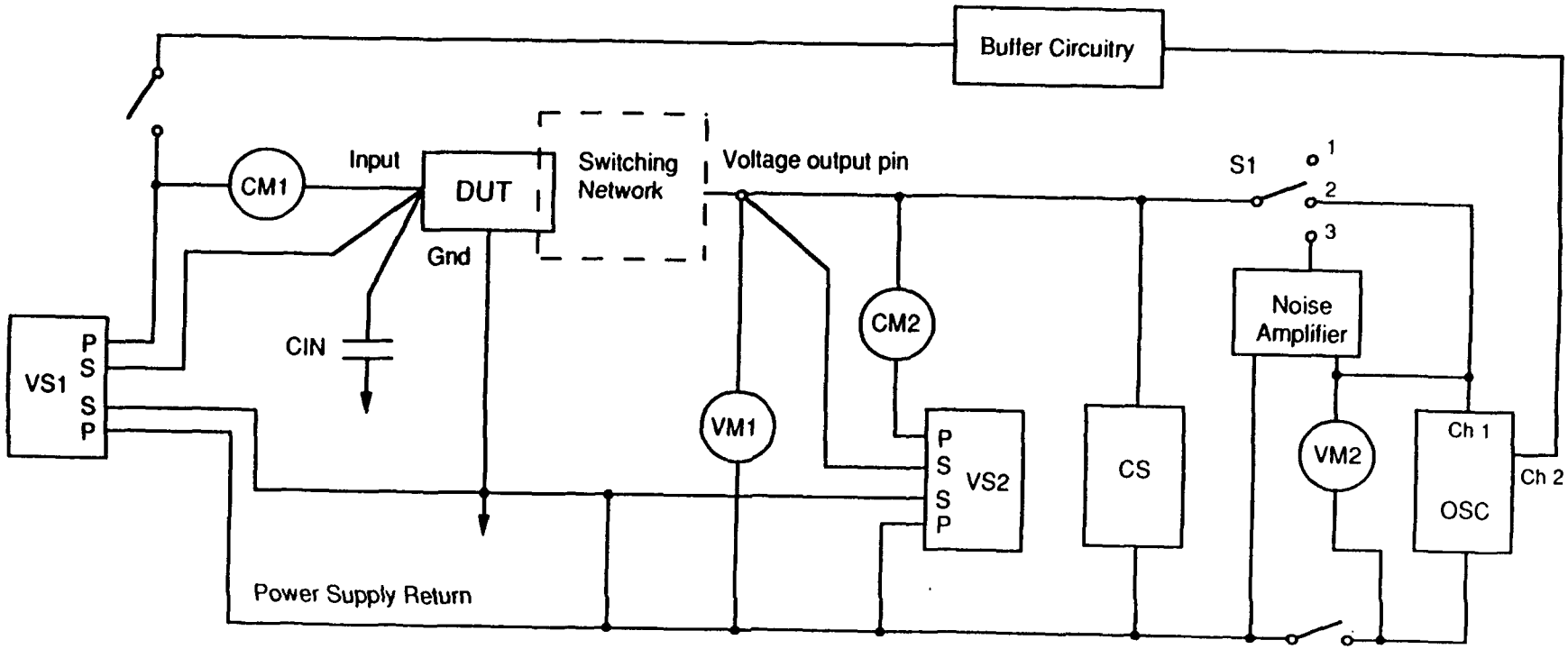
4.0 SUMMARY. The following details shall be specified in the applicable procurement document.

a. Specified values for V_{IN}, I_L and V_{OUT} for all tests.
b. Input and output capacitor values (C_I and C_L).
c. Delay between V_{OUT} measurements for VR_{LOAD} and VR_{LINE} tests.
d. Pulse duration and t_{OSS} for I_{OS} test.
e. t_{PS} error band.
f. Test limits for all parameters.
g. Temperature limits for output voltage temperature coefficient test.
h. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.

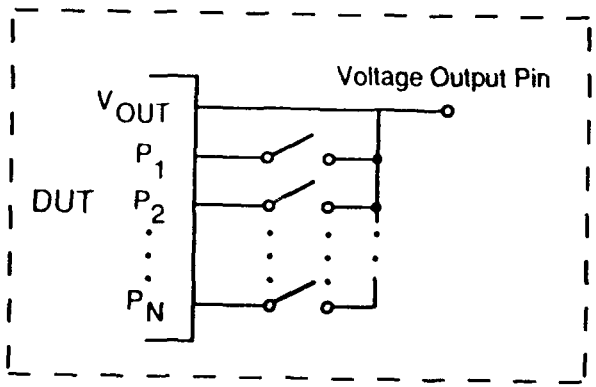
Parameter	Input Voltage VS_1	Load Current CS	Load Voltage VS_2	Switch S1	Measurement Meter	Measurement Value	Equation	Units	Notes
V_{OUT}	V_{IN}	I_L	OPEN	Pos. 1	VM1	E_1	$V_{OUT} = E_1$	Volts	See Note 1
VR_{LOAD}	V_{IN} V_{IN}	I_{L1} I_{L2}	OPEN OPEN	Pos. 1 Pos. 1	VM1 VM1	E_2 E_3	$VR_{LOAD} = E_3 - E_2$	Volts	See Note 1 See fig. 2
VR_{LINE}	V_{IN1} V_{IN2}	I_L I_L	OPEN OPEN	Pos. 1 Pos. 1	VM1 VM1	E_4 E_5	$VR_{LINE} = E_5 - E_4$	Volts	See Note 1 See fig. 2
I_{OS}	V_{IN}	OPEN	0.0V	Pos. 1	CM2	I_1	$I_{OS} = I_1$	Amps	See fig. 2
I_Q	V_{IN}	OPEN	OPEN	Pos. 1	CM1	I_2	$I_Q = I_2$	Amps	
t_{ps}	V_{IN}	OPEN	OPEN	Pos 2.	Scope	t_1	$t_{ps} = t_1$	Sec.	See fig. 2
N_O	V_{IN}	OPEN	OPEN	Pos. 3	VM2	E_6	$N_O = E_6$	V_{RMS}	See Note 2
N_O	V_{IN}	OPEN	OPEN	Pos. 3	Scope	E_7	$N_O = E_7$	Volts	See Note 3

Note 1: For pin programmable references, measurements may be required for each specified voltage output level.
Note 2: Test conditions for high frequency noise measurement.
Note 3: Test conditions for low frequency noise measurement.

Table 1. Equations for voltage reference parameters

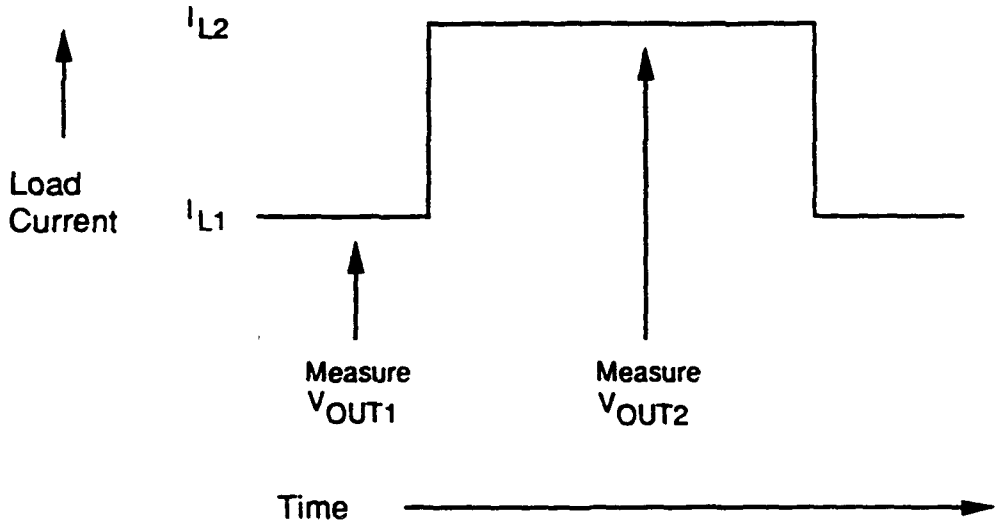


Voltage Reference Test Circuit

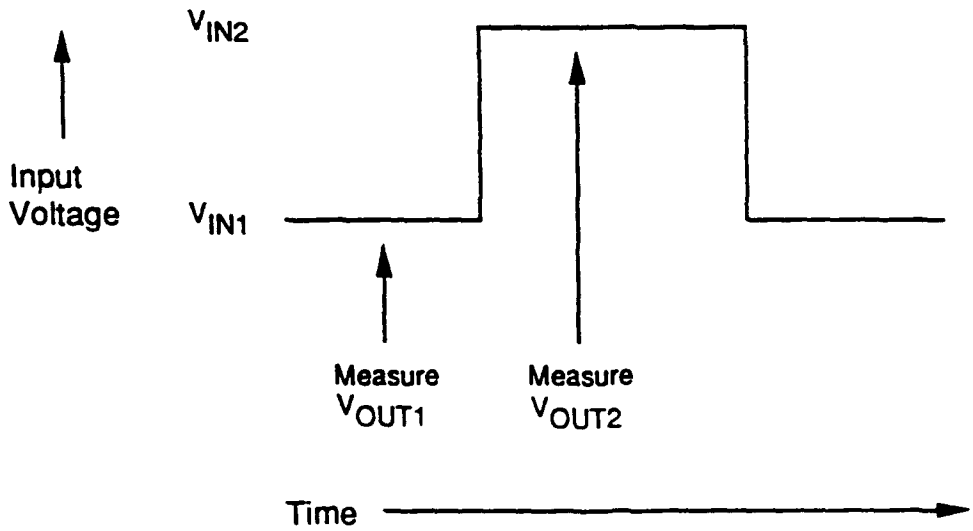


Sample switching network for pin programmable reference

Figure 1. Voltage Reference Test Circuit

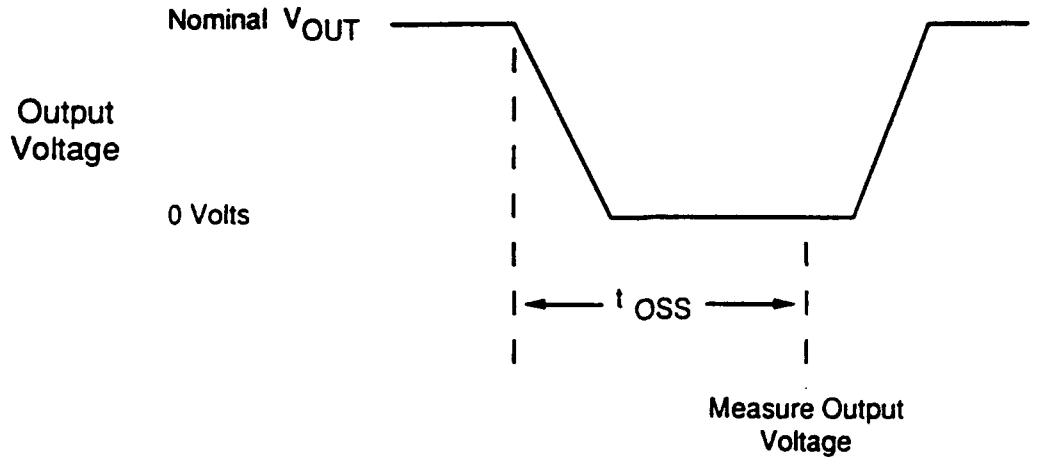


Load Regulation Waveform Diagram

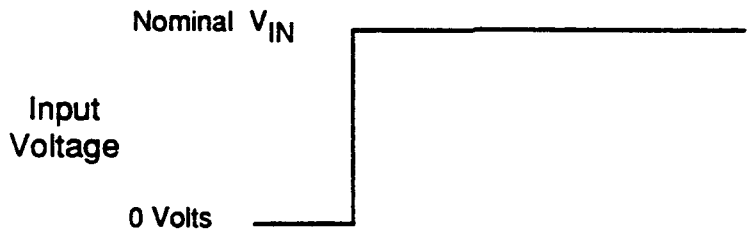


Line Regulation Waveform Diagram

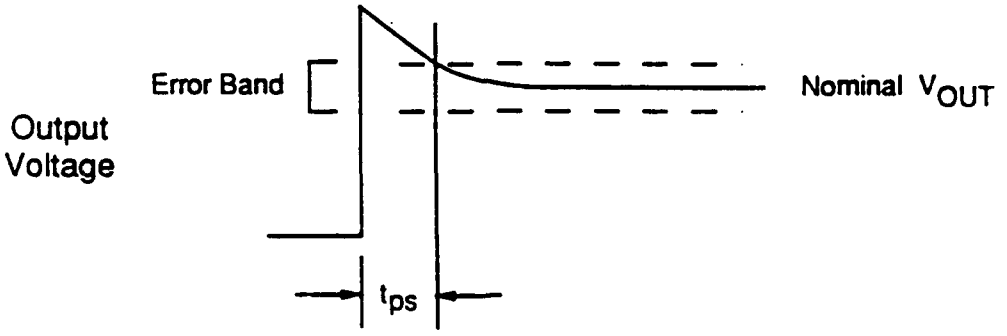
Figure 2. Voltage Reference Waveforms



Short Circuit Output Current Waveform Diagram



Note: Rise time of input pulse specified in procurement document



Turn-on Settling Time Voltage waveforms

Figure 2. Voltage Reference Waveforms (cont.)

METHOD 4004

LINEAR VOLTAGE REGULATOR STATIC PARAMETERS

1.0 PURPOSE. This method establishes the means for measuring output voltage, load regulation, line regulation, standby current, adjust pin current, output short circuit current, minimum load current, thermal voltage, output noise, ripple rejection ratio and start-up voltage of monolithic silicon, three-terminal fixed and adjustable, positive and negative linear voltage regulators.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Output Voltage (V_{OUT}). The regulated voltage at the output of the voltage regulator referenced to the external zero reference level of the supply voltage (ground or adjust pin as specified).

1.1.2 Supply Voltage (V_{LINE}). The voltage supplied at the input of the voltage regulator.

1.1.3 Input Voltage Range. The range of input supply voltage over which the regulator will operate. For an adjustable regulator, this is usually a range of V_{IN} - V_{OUT} differential voltage.

1.1.4 Output Voltage Range. The range of output voltage over which the regulator will operate.

1.1.5 Line Regulation (VR_{LINE}). The change in output voltage for a specified change in input voltage under a constant load condition.

1.1.6 Load Regulation (VR_{LOAD}). The change in output voltage for a specified change in the load current under a constant input voltage.

1.1.7 Standby Current Drain (I_{SCD}). The supply current drawn by the regulator with no load or with a specified high resistance load. This parameter applies to fixed regulators only.

1.1.8 Output Short Circuit Current (I_{OS}). The current from the output of the voltage regulator when the output is at zero volts (ground).

1.1.9 Minimum Load Current (I_{MIN}). The minimum current at which the voltage regulator will regulate the output voltage. This parameter applies to adjustable regulators only.

1.1.10 Voltage Start-up (V_{START}). The voltage at the output of the regulator subsequent to a step in input voltage from zero volts to nominal input voltage. V_{START} is measured at a specified time after initiation of the change in input voltage.

1.1.11 Output Noise (N_O). The rms noise voltage output from the regulator for a specified DC input voltage.

1.1.12 Ripple Rejection Ratio (R_{RR}). The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

1.1.13 Thermal Regulation (V_{RTH}). The change in output voltage at a specified input voltage after increasing the load current from minimum to a specified value and waiting a specified time. The change in output voltage is due to thermal effects and is specified as a function of power dissipation in the DUT.

1.1.14 Adjust Pin Current (I_{ADJ}). The current required at the adjust pin of adjustable voltage regulators.

2.0 APPARATUS. The apparatus shall consist of programmable voltage sources, a programmable current source and programmable resistive voltage dividers, voltmeters and current meters, resistors and capacitors to implement the circuits of figures 1, 3 and 4.

2.1 DC Voltmeter (VM1). The voltmeter used to measure the output voltage of the regulator under test should be accurate to 0.05% over the range of output voltages of the regulator. The response time of the voltmeter to a change in voltage will be equal to or better than 0.1 times the minimum time specified for the voltage regulator to respond to changes in line voltage and load current, i.e., if the regulator is specified to respond within 1 ms the voltmeter should be capable of responding within 0.1 ms. The voltmeter will be programmable to make a measurement at a specified interval after the application of a strobe coincident with programmed changes in line voltage or load current.

2.2 AC Voltmeter (VM2). The AC voltmeter used to measure noise voltage and ripple voltage of the regulator under test should measure true rms voltage to an accuracy of 1.0% over the bandwidth from 10 HZ to 10 KHZ.

2.3 DC Current Meters (CM1, CM2). Programmable current meters are required to measure output short circuit current and standby or adjustment current. The current meters should be accurate to 0.1% over the range of current to be measured. Additionally, the current meter used to measure the short circuit output current must be programmable to make a current measurement at a specified time following the application of the short circuit voltage condition at the output of the regulator under test.

2.4 Programmable Input Voltage Supply (VS_1). The programmable input voltage supply will be capable of forcing positive or negative voltage to a resolution of 0.1% and with an accuracy of 0.05% over the range of input voltage and current specified for the regulator under test. The input voltage supply will be capable of providing a voltage pulse of duration specified in the voltage regulator procurement document. The input voltage supply will be provided with separate sense and power inputs/outputs.

2.5 Programmable Output Voltage Supply (VS_3). The function of the output voltage supply is to simulate a transient short circuit at the output of the regulator in test. The output voltage supply will be capable of changing under program control from a voltage level equal to the nominal output voltage of the regulator under test to a the ground reference level of the regulator and back to nominal level in an interval specified in the

procurement document as being short enough to prevent thermal damage to the regulator in test. A programmable open mode will enable the equivalent of switching the output voltage supply out of the regulator load path. The output voltage source will be programmable to an accuracy of 0.1% of the nominal output voltage of the regulator and will be capable of sourcing or sinking current greater than the maximum short circuit current specified for the regulator in test. Separate sense and power inputs/outputs will be provided.

2.6 Programmable Output Current Supply (CS). The programmable output current supply will be capable of sourcing or sinking current to an accuracy of 1.0% over the range of output currents specified for the regulator in test. The output current supply will be programmable to generate a current pulse of amplitude and width specified for measurement of load regulation of the regulator in test.

2.7 Programmable Standby Voltage Supply (VS_2). The programmable standby voltage supply will be capable of forcing positive or negative voltage to a resolution of 0.1% and with an accuracy of 0.05% over the range of input voltage and current specified for the regulator in test. The standby voltage supply will be provided with separate voltage sense and power inputs/outputs.

2.8 Sine Wave Generator (VS_4). The sine wave generator shall be capable of generating a 5 volt rms sine wave variable in frequency from 10 Hz to 10 kHz.

2.9 Programmable Voltage Divider (VD). For the purpose of this specification, a programmable voltage divider implements a resistive voltage divider consisting of two resistors connected in series with a center tap. The value of each resister in the voltage divider is programmable, i.e., switch selectable manually or automatically under control of a computer/ controller device. Resistor values will depend on the device in test and may include zero resistance or open circuit. Resistors in voltage divider networks shall be accurate to within 1.0%.

2.10 DC voltage and AC voltage Summing Circuit. A summing circuit is required to sum the DC and AC voltages at the input terminal of the regulator for the ripple voltage test.

2.11 Load Resistor (R_L). A load resistor is required to perform the V_{START} test. The value of this resistor will be specified in the procurement document.

3.0 PROCEDURE. Figure 1 shows the generic test configuration for three terminal fixed and adjustable voltage regulators. Figure 3 illustrates a special test circuit to be used for the output noise test, and figure 4 shows the special circuit used for ripple rejection testing. Procedures for specific tests are described below and summarized in Table 1.

3.1 Output Voltage (V_{OUT}). The regulated output voltage from the device in test is measured at the output pin of the regulator with voltmeter VM1. The input voltage supply (VS_1) is set to the specified input voltage, V_{IN}, the load current supply (CS) is set to the specified load current, I_L, and

the short circuit current voltage supply is set to the open condition. If the regulator is of the adjustable type, the control pin voltage supply (VS_2) is set to the specified condition and the voltage divider (VD) is set to the specified values. If the regulator is of the fixed voltage type, resistor R_A of the voltage divider is programmed open and VS_2 is programmed to the regulator ground.

3.2 Load Regulation (VR_{LOAD}). Load regulation is obtained from two measurements of V_{OUT} at two different values of load current specified in the procurement specification. V_{OUT} is measured at an initial load current, I_{L1}, the load current supply is then switched to a value I_{L2} and V_{OUT} is measured at a specified time after the current transition to level I_{L2} as shown in the waveform diagrams of figure 2. Load regulation is calculated as:

$$VR_{LOAD} = E_2 - E_1$$

where E_1 is the initial output voltage level for load current I_{L1} measured at VM1 and E_2 is the output voltage measured by VM1 after the transition to I_{L2}.

3.3 Line Regulation (VR_{LINE}). Line regulation is obtained from two measurements of V_{OUT} at two different values of line voltage, V_{IN}, as specified in the procurement specification. During this test, current supply CS must provide a constant load current greater than the minimum load current specified for the regulator under test. V_{OUT} is measured at an initial line voltage V_{IN1}, the line voltage supply, VS_1, is pulsed to a value V_{IN2} and V_{OUT} is measured by voltmeter VM1 at a specified time after the input voltage transition to V_{IN2} takes place as shown in the waveform diagrams of figure 2. Line regulation is calculated as:

$$VR_{LINE} = E_2 - E_1$$

where E_1 and E_2 are the output voltages measured by VM1 for specified line voltages V_{IN1} and V_{IN2}.

3.4 Standby Current Drain (I_{SCD}). Standby current drain of fixed voltage regulators is measured at the control pin output with current meter CM1. Line voltage and load current are set to specified levels and the standby current voltage supply is set to maintain the control pin voltage level at the ground reference level of the regulator in test.

3.5 Adjust Pin Current (I_{ADJ}). Adjust pin current of adjustable voltage regulators is measured at the adjust pin with current meter CM1. For this measurement the voltage divider, VD, is disconnected from the output of the regulator by programming resistor R_A to be open. Line voltage and load current are set to specified voltages and the standby current voltage supply is set to maintain the adjust pin voltage level at ground.

3.6 Short Circuit Output Current (I_{OS}). The short circuit current is measured by current meter CM2 while the output of the regulator is pulsed to ground return voltage level by the output voltage supply, VS_3. The measurement is made at a time, t_{OSS}, after the initiation of the voltage pulse at the output of the regulator (see the waveforms of figure 2).

Duration of the pulse, t_{OSS}, input voltage to the regulator and voltage at the control or adjustment pin will be as specified in the procurement document.

3.7 Minimum Load Current (I_{MIN}). To measure minimum load current the output pin of the regulator is forced to a specified voltage using VS_3 and current measured at current meter CM2. Input voltage supplied by VS_1, and the resistor values of VD will be specified in the procurement document. Supplies VS_2 and CS are programmed open for this test.

3.8 Voltage Start-up (V_{START}). Start-up voltage is measured at the output of the regulator by voltmeter VM1. The input voltage supply, VS_1, is switched from zero volts to a specified value of V_{IN} and the output voltage is measured at a specified time, t_{START}, after the initiation of the input voltage transition (see the waveforms of figure 2). A load resistor R_L, is programmed to a specified value and the control/adjustment pin is biased as specified by either the voltage supply, VS_2, or the divider, VD.

3.9 Thermal Voltage (V_{TH}). With the regulator in test operating with minimum load current, the output voltage of the regulator is measured with voltmeter VM1 to verify correct operation. The output load current is set to specified load current IL_{MAX}. Output voltages V_1 and V_2 are then measured at specified times t1 and t2.

$$V_{RTH} = V_2 - V_1$$

3.10 Output Noise (N_O). Output noise is measured with the test circuit of figure 3. With the specified voltage applied to the input of the regulator, the rms noise voltage is measured with voltmeter VM2 which has a specified bandwidth.

3.11 Ripple Rejection Ratio (R_{RR}). Ripple rejection ratio is measured with the test circuit of figure 4. The DC input voltage is applied at the DC voltage input pin and the AC voltage at the AC voltage input to provide input ripple voltage at a specified voltage level. The output rms voltage is then measured by VM2 at the output terminal under specified load conditions. The bandwidth of the rms voltmeter shall be from 10HZ to 10KHZ.

$$\text{Ripple Rejection(db)} = 20 \text{ LOG} \left(\frac{E_O}{E_i} \right) \quad \text{db}$$

where E_O = output ripple voltage
E_i = input ripple voltage

4.0 SUMMARY. The following details shall be specified in the applicable procurement document.

a. Resistor values for R_A and R_B where necessary.
b. Input and output capacitor values (C_I and C_L).
c. V_{IN}, I_L, and V_{OUT} for each test.
d. Time between measurements for VR_{LOAD} and VR_{LINE} tests.
e. Values for t_{OSS} and t_{START}.
f. Frequency range for noise test.
g. t_1 and t_2 for thermal voltage measurement.
h. Input DC and AC voltage for ripple rejection test circuit.
i. Frequency of AC voltage for ripple rejection test.
j. Test limits for each parameter measured.
k. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.

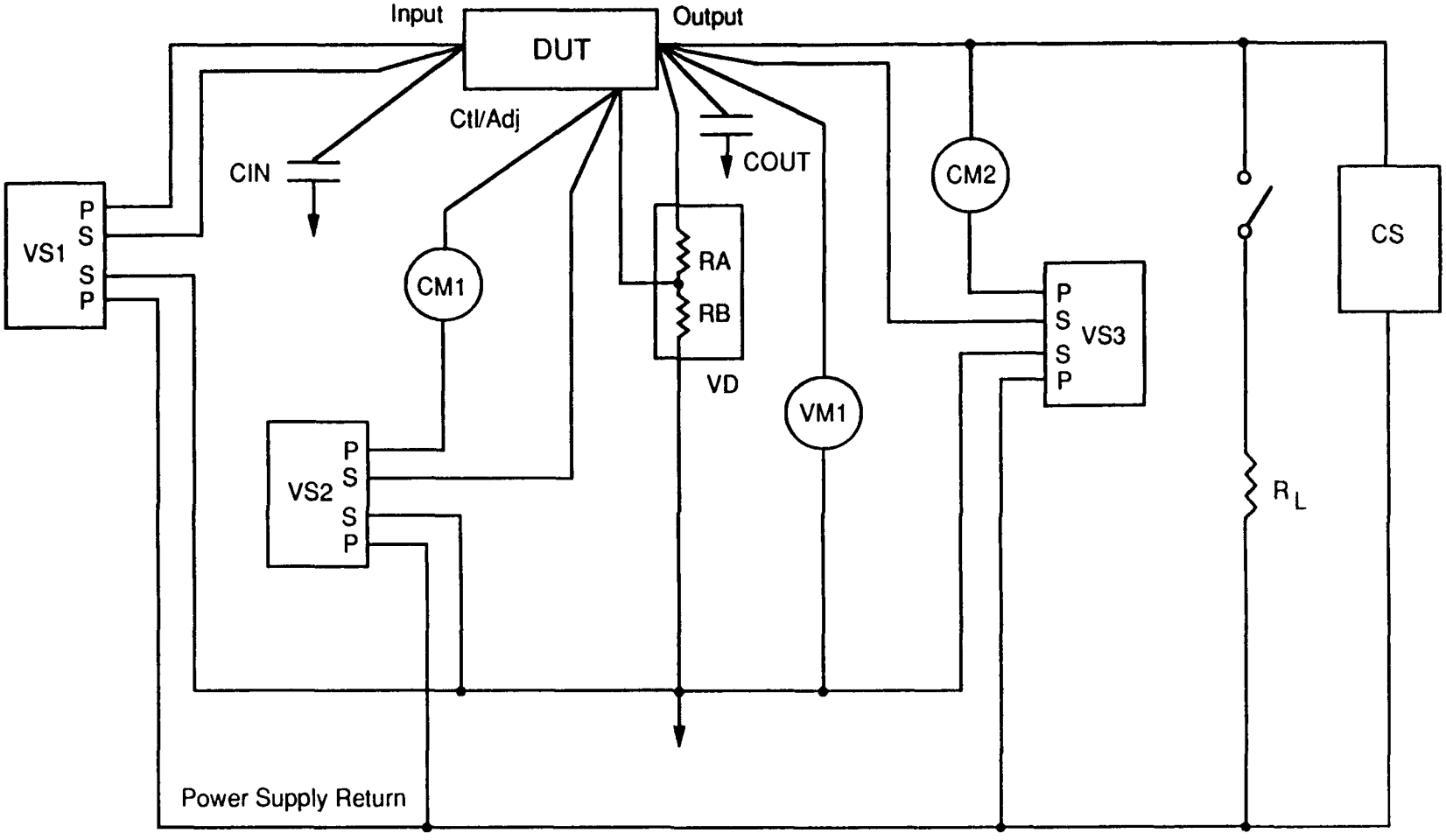
Parameter	Input Voltage VS_1	Control Voltage VS_2	Load Current CS	Load Voltage VS_3	Voltage Divider VD	Measurement		Equation	Units	Notes
						Meter	Value			
V_{OUT}	V_{IN}	0V (Fixed) OPEN (Adj)	I_L	OPEN	OPEN (Fixed) R_A/R_B (Adj)	VM1	E_1	$V_{OUT} = E_1$	Volts	See Fig. 2
VR_{LOAD}	V_{IN}	0V (Fixed) OPEN (Adj)	I_{L1} I_{L2}	OPEN	OPEN (Fixed) R_A/R_B (Adj)	VM1	E_2 E_3	$VR_{LOAD} = E_3 - E_2$	Volts	See Fig. 2
VR_{LINE}	V_{IN1} V_{IN2}	0V (Fixed) OPEN (Adj)	I_L	OPEN	OPEN (Fixed) R_A/R_B (Adj)	VM1	E_4 E_5	$VR_{LINE} = E_5 - E_4$	Volts	See Fig. 2
I_{SCD}	V_{IN}	0V (Fixed) N/A (Adj)	I_L	OPEN	OPEN	CM1	I_1	$I_{SCD} = I_1$	Amps	Fixed Regulators
I_{ADJ}	V_{IN}	N/A (Fixed) 0V (Adj)	I_L	OPEN	OPEN	CM1	I_2	$I_{ADJ} = I_2$	Amps	Adjustable Regulators
I_{OS}	V_{IN}	0V (Fixed) OPEN (Adj)	OPEN	0.0V	OPEN (Fixed) R_A/R_B (Adj)	CM2	I_3	$I_{OS} = I_3$	Amps	See Fig. 2
I_{MIN}	V_{IN}	N/A (Fixed) 0V (Adj)	OPEN	V_{OUT}	OPEN (Fixed) R_A/R_B (Adj)	CM2	I_4	$I_{MIN} = I_4$	Amps	Adjustable Regulators See Note 1
V_{START}	V_{IN} (PULSE)	0V (Fixed) OPEN (Adj)	Use R_L	OPEN	OPEN (Fixed) R_A/R_B (Adj)	VM1	E_6	$V_{START} = E_6$	Volts	See Fig. 2

Table 1. Three Terminal Linear Voltage Regulator Equations

Parameter	Input Voltage VS_1	Control Voltage VS_2	Load Current CS	Load Voltage VS_3	Voltage Divider VD	Measurement		Equation	Units	Notes
						Meter	Value			
N_O	V_{IN}	0V (Fixed) OPEN (Adj)	Use R_L	OPEN	OPEN (Fixed) R_A/R_B (Adj)	VM2	E_7	$N_O = E_7$	Volts	See Fig. 3
R_{RR}	V_{IN} V_{AC}	0V (Fixed) OPEN (Adj)	Use R_L	OPEN	OPEN (Fixed) R_A/R_B (Adj)	VM2	E_8	$R_{RR} = 20 \log[E_8/V_{AC}]$	Volts	See Fig. 4
V_{RTH}	V_{IN}	0V (Fixed) OPEN (Adj)	$I_{L(MIN)}$ $I_{L(MAX)}$	OPEN	OPEN (Fixed) R_A/R_B (Adj)	VM1	E_9 E_{10}	$V_{RTH} = E_{10} - E_9$	Volts	

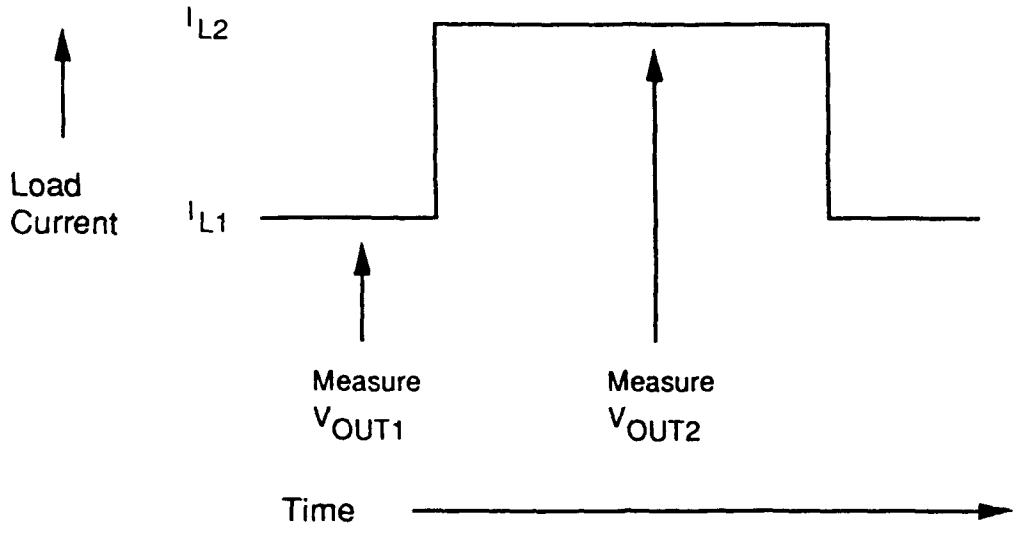
Note 1: V_{OUT} for I_{MIN} test is specified in procurement document
Note 2: V_{AC} is input ripple voltage supplied by VS_4

Table 1. Three Terminal Linear Voltage Regulator Equations (cont)

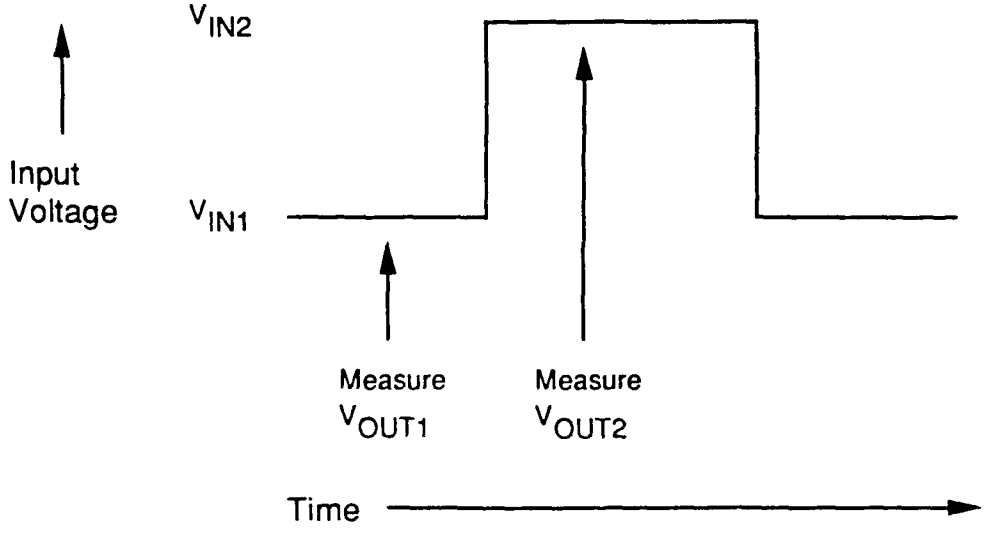


Note: R_L used for V_{START} test only.

Figure 1. Test Circuit for 3-Terminal Linear Voltage Regulators

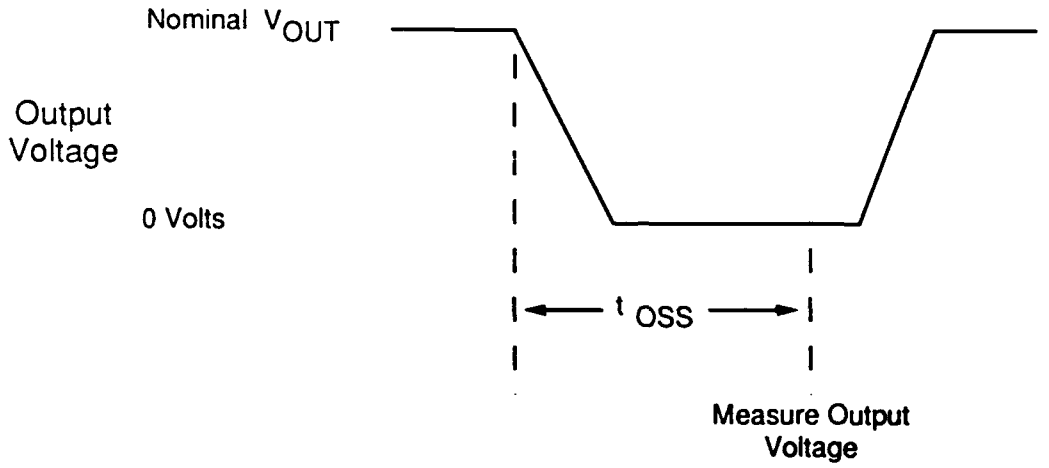


Load Regulation Waveform Diagram

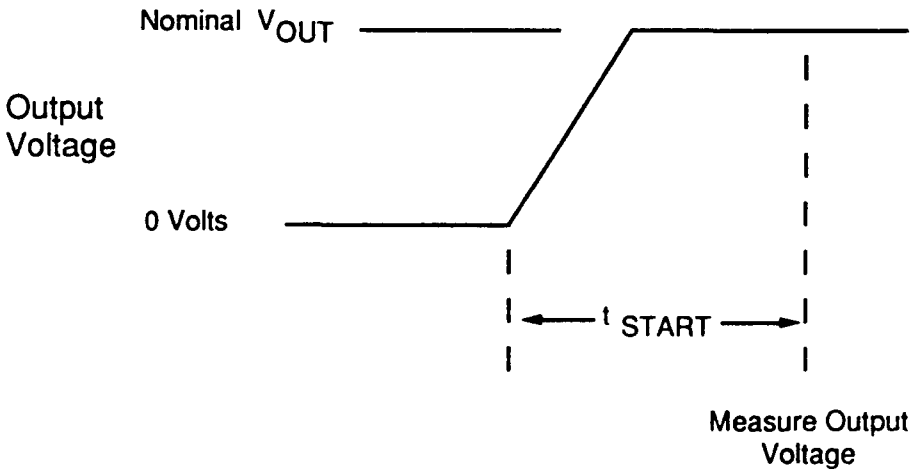


Line Regulation Waveform Diagram

Figure 2. Linear Voltage Regulator Waveforms

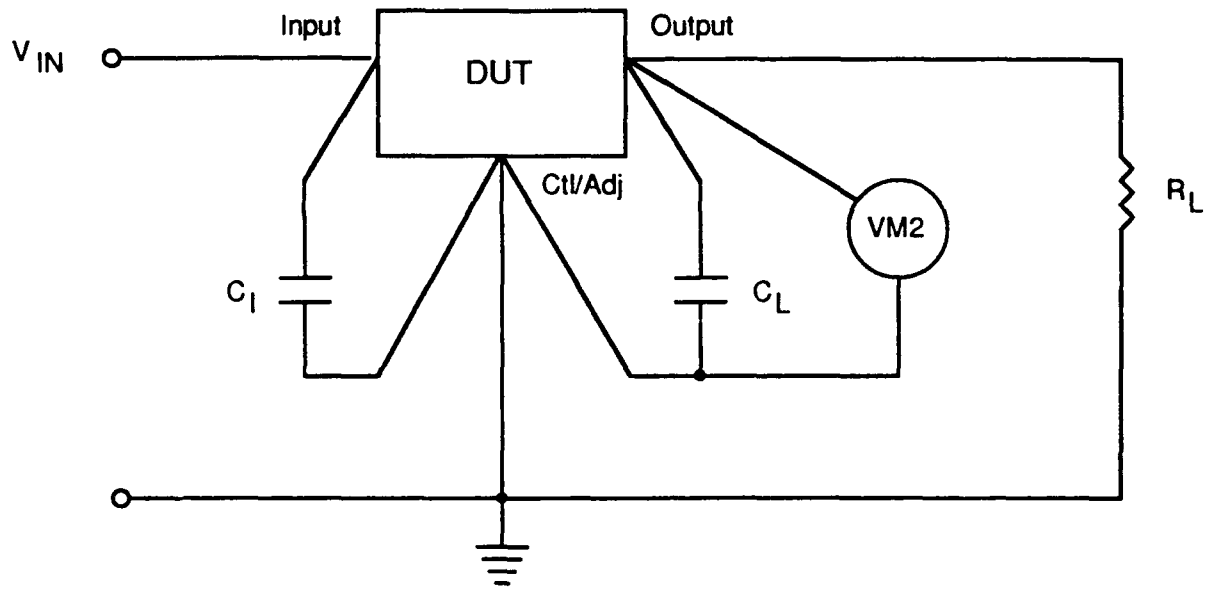


Short Circuit Output Current Waveform Diagram



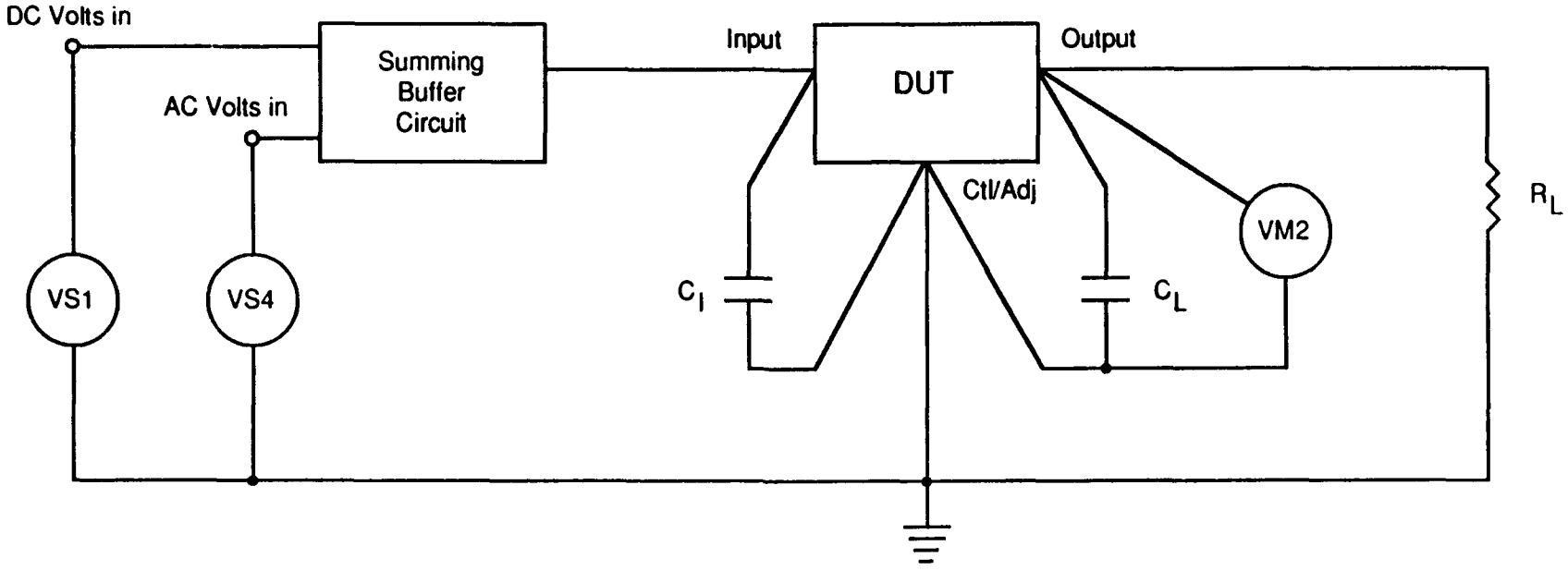
Voltage Start-up Waveform Diagram

Figure 2. Linear Voltage Regulator Waveforms (cont.)



Note: Output load will be specified in procurement document

Figure 3. Output Noise Test Circuit



Notes: 1. Summing buffer circuit accepts dc voltage and ac voltage inputs to provide a dc level with superimposed ac ripple at DUT input.

2. Input capacitor Ci shall be minimum value to prevent oscillations of the DUT

3. The meter for measuring output voltage shall have a minimum bandwidth from 10 Hz to 10 kHz and shall measure true rms voltages

Figure 4. Ripple Rejection Test Circuit

METHOD 4005

SAMPLE AND HOLD AMPLIFIER TEST METHODS

1.0 PURPOSE. This method establishes the means for measuring input offset voltage, input bias current, gain error, feedthrough rejection ratio, hold mode droop voltage rate, hold step voltage, input leakage current, power supply current, power supply rejection ratio, acquisition time, aperture time, transient response, and noise for integrated circuit sample-and-hold amplifiers (S/H amplifiers). The method is also applicable to track-and-hold amplifiers. The method applies to both inverting type and non-inverting types and to types having either internal or external hold capacitors.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Full Scale Voltage (FS). The maximum positive (+FS) and negative (-FS) input voltages that can be applied to the S/H amplifier.

1.1.2 Input Offset Voltage (V_{IO}). The difference between the input and output voltages in the sample mode for a specified common mode voltage condition.

1.1.3 Input Offset Voltage Drift (DV_{IO}). Input offset voltage drift is the ratio of the change of input offset voltage (ΔV_{IO}) to the change in circuit temperature (ΔT).

$$DV_{IO} = \frac{\Delta V_{IO}}{\Delta T}$$

1.1.4 Input Offset Voltage Adjustment Range ($V_{IO}(adj+)$, $V_{IO}(adj-)$). The input offset voltage adjustment ranges are the differences between the offset voltage (V_{IO}) measured with the voltage adjust terminal open circuited, and the offset voltage measured with the maximum positive or negative voltage applied to the voltage adjust terminal.

1.1.5 Input Bias Current (I_{IB}). The current flowing into the signal input for any specified common mode voltage condition.

1.1.6 Hold Mode Leakage Current ($I_{HL}(+)$, $I_{HL}(-)$). The input bias current of the output buffer amplifier. This leakage current causes a droop rate error of the external hold capacitor.

1.1.7 Hold Step Voltage (V_{HS}). The output voltage change with a fixed input voltage when the device is switched from the sample to hold mode with a specified logic signal.

1.1.8 Gain Error (A_E). The ratio of sample mode output voltage swing to input common mode voltage swing expressed in percent. This may be interpreted as the percentage deviation from unity gain.

1.1.9 Feedthrough Rejection Ratio (F_{RR}). The ratio in decibels of an input voltage change to a hold mode output voltage change.

1.1.10 Hold Droop Rate (DR(+), DR(-)). The rate of change of the hold capacitor voltage with time due to hold mode leakage current.

1.1.11 Acquisition Time (t_{aq}). The minimum sample time required for the sample-and-hold amplifier to acquire a full scale voltage change to within a specified error band of final value for a specified hold capacitor size.

1.1.12 Aperture Time (t_{ap}). The delay time necessary between a hold command signal and a specified voltage step on the input to ensure that the voltage step does not cause the held output voltage to change by more than a specified amount.

1.1.13 Transient Response Time (TR_{ts}). The time after the application of a specified input voltage pulse for the amplifier to settle to within a specified error band of final value.

1.1.14 Transient Response Overshoot (TR_{os}). The greatest deviation of the output voltage from the final value that occurs in response to a specified input pulse.

1.1.15 Power Supply Rejection Ratio (PSRR). The power supply rejection ratio is the ratio of the change in input offset voltage, V_{IO}, to the corresponding change in one power supply voltage with all remaining power supply voltages held constant.

$$PSRR+ = \frac{\Delta V_{IO}}{\Delta(+V_{CC})} \qquad -V_{CC} = \text{constant}$$

$$PSRR- = \frac{\Delta V_{IO}}{\Delta(-V_{CC})} \qquad +V_{CC} = \text{constant}$$

The power supply rejection ratio can also be expressed in terms of open loop gain, A_D, change in output voltage, V_O, and corresponding change in power supply voltage, $+V_{CC}$ or $-V_{CC}$.

$$PSRR = \frac{\Delta V_O}{A_D * \Delta V_{CC}}$$

1.1.16 Noise. The total noise (No) that exists within a 10 HZ to 10 KHZ "brickwall" bandwidth. This measurement is made with the device under test in "sample" mode, $en_{(S)}$, and "hold" mode, $en_{(H)}$.

2.0 APPARATUS. The apparatus shall consist of a precision voltage source, a precision voltmeter, an oscilloscope or other means for measuring time delays, a sine wave voltage generator, an ac voltmeter and a pulse generator to implement the circuits in figures 1, 4 and 5.

2.1 Programmable Voltage Source. The voltage source used to provide an input voltage signal to the test device shall be programmable over the range of +15 to -15 volts and shall be accurate to 0.1%.

2.2 Programable Logic Voltage Source. The logic voltage source used to provide a control signal to the control inputs of the test device shall be programmable to provide a logic voltage between 0 volts and 5.5 volts for TTL inputs or -2.0 volts to 0.0 volts for ECL inputs, with an accuracy of 0.01 volts. The logic voltage source shall be capable of generating a pulsed output with pulse width programmable from 0.1 μs to 1 ms.

2.3 Voltage Measurement System. The voltage measurement system shall be a sample-and-hold type having programmable delay in response to an external trigger of 1 to 100 μs. Alternatively, a continuous reading voltmeter may be used providing that a sample-and-hold amplifier is connected at the output of the error amplifier of figure 1, and suitable trigger pulse generating circuitry is provided. The voltage measurement system will be accurate to 0.1%.

2.4 Power Supplies. The device power supplies will be capable of providing amplifier and logic supply voltages required by the device specification.

2.5 Hold Capacitor. If an external hold capacitor is required by the test device it shall be of the teflon type or other linear and stable materials.

2.6 Pulse Generator. The pulse generator for generating the input pulse for the transient response test shall be capable of driving the analog input of the amplifier with a 100 mv amplitude pulse having a rise time of 50 ns or faster.

2.7 Oscilloscope. The oscilloscope or sampling voltmeter for observing the output pulse of the transient response test shall be capable of a sampling rate of 10 million samples/sec with a sensitivity of 10 mv/cm.

2.8 RMS Voltmeter (VM). The rms voltmeter used to measure wideband noise should have a bandwidth of 5 HZ to 20 kHz or higher and be capable of measuring rms voltage to an accuracy of 0.1mv.

3.0 PROCEDURE. Figure 1 shows the generic test circuit for sample-and-hold amplifier tests. The test approach uses an error amplifier to compare the input and output voltage levels of the S/H amplifier in test. For non-inverting types of S/H amplifiers, switch S1 is placed in position 1 and for inverting types in position 2. With relay K1 in the normal state, the error amplifier amplifies the output of the DUT with a gain of 100. With K1 activated, the error amplifier will amplify the difference between the input voltage and the output voltage of the DUT by 100. Relay K_2 inserts a 100 KΩ resistor at the input of the S/H amplifier for the purpose of measuring input current. Relay K_4 is used in the calibration measurement. Additional test circuits are shown in figures 4 and 5. The circuit in figure 4 is used to measure transient response time and transient response overshoot, while figure 5 illustrates the noise test circuit.

3.1 Error Amplifier Calibration Voltage (V_{CAL}). The error amplifier will have its own offset voltage which must be subtracted when measuring the offset voltage of the S/H amplifier (V_{IO}). For other measurements in this test procedure, the result is calculated as the difference of two output voltages, and thus in these cases the error amplifier offset will cancel out.

To obtain V_{CAL}, the output voltage, E_1, at the error amplifier output terminal of the test circuit is measured with no device present in the test socket and with relays K_1 and K_4 actuated (amplifier inputs grounded through 1 KΩ). If the circuit is to be used to test an inverting S/H amplifier, the measurement is made with switch S_1 in the position shown in figure 1, and the value of V_{CAL} is equal to $E_1/200$. If a non-inverting S/H amplifier is to be tested the switch is closed to the alternate contacts and the value of V_{CAL} will be equal to $E_1/100$.

3.2 Input Offset Voltage (V_{IO}). With V_{IN} equal to zero volts and relay K_1 actuated, the voltage, E_2, at the output of the test circuit is measured. V_{IO} for the S/H amplifier is then calculated as:

$$V_{IO} = \frac{E_2 - E_1}{100} \quad \text{volts}$$

3.3 Input Offset Voltage Drift (DV_{IO}). Measurement of V_{IO1} is made at temperature T_1 as described in section 3.2, and a second measurement of V_{IO2} is made at the second temperature (T_2). DV_{IO} is then calculated as:

$$DV_{IO} = \frac{V_{IO2} - V_{IO1}}{T_2 - T_1}$$

3.4 Input Offset Voltage Adjustment Range ($V_{IO}(adj)$). The input offset voltage adjust is determined by first measuring input offset voltage (V_{IO}) using the procedure in section 3.2. Two additional values are then required. $V_{IO}(+)$ is determined by measuring with the maximum positive voltage applied to the adjust terminal. $V_{IO}(-)$ is found similarly except the maximum negative voltage is applied to the adjust terminal. The following equations are then used:

$$V_{IO}(adj+) = V_{IO} - V_{IO}(+)$$

$$V_{IO}(adj-) = V_{IO} - V_{IO}(-)$$

3.5 Input Bias Current (I_{IB}). With relays K_1 and K_2 actuated, and zero volts at the input, the voltage E_3 at the error amplifier output is measured. I_{IB} is calculated using the value of E_2 measured as in section 3.2 and the value of the input resistance.

$$I_{IB} = \frac{E_2 - E_3}{100{,}000} \quad \text{amperes}$$

3.6 Hold Step Voltage (V_{HS}). This measurement is made with relay K_1 actuated. A specified input voltage is applied to the S/H amplifier and it is switched from sample to hold state with a specified logic signal. The error voltages before and after the transition are compared. The time after the application of the logic signal for the hold state error voltage measurement will be specified in the procurement document and should be approximately twice the settling time of the amplifier. V_{HS} is calculated from the following equation:

$$V_{HS} = \frac{E_5 - E_4}{100} \qquad \text{volts}$$

where E_4 is the error voltage in the sample mode and E_5 the error voltage in the hold mode.

3.7 Gain Error (A_E). To measure gain error, +FS volts then -FS volts is applied at the input of the S/H amplifier with relay K_1 actuated. The error amplifier output voltages, E_6 and E_7 respectively, are measured. The change in output voltage measured at the error amplifier output is compared with the output at zero volts in to obtain the gain error as a percentage. In the equation below, the error amplifier output voltages E_6 and E_7 have been divided by 100 to obtain the output at the amplifier in test and the fraction has been multiplied by 100 to obtain a percent.

$$A_E = \frac{E_6 - E_7}{(+FS) - (-FS)} \qquad \%$$

3.8 Feedthrough Rejection Ratio (F_{RR}). F_{RR} is measured for a dc step voltage at the input while the amplifier in test is in the hold mode. A specified input voltage is applied while the amplifier in test is in the sample mode and the amplifier is then switched to the hold mode. The error amplifier output voltage, E_8, which will include the effect of hold step voltage, is measured. The input voltage to the device in test is then stepped to a specified voltage level and the new error amplifier output voltage, E_9, is measured. The magnitude of the voltage step, ΔV_{IN}, is compared to the change in output voltage of the test amplifier to obtain F_{RR}:

$$F_{RR} = 20*\log\left(\frac{100\Delta V_{IN}}{E_9 - E_8}\right) \qquad \text{db}$$

3.9 Hold Droop Rate (DR(+), DR(-)). This measurement is made with relay K_1 actuated. DR(+) is measured with +FS volts at the input of the S/H amplifier and DR(-) with -FS volts at the input. The amplifier is switched from sample to hold mode and two measurements of error voltage are made at times t_1 and t_2 after switching. The time of the first measurement, t_1, may be specified in the procurement document and should be approximately twice the aperture time. The interval between the two measurements should be specified in the procurement document. A shorter interval time may be specified for 125° C measurements owing to higher leakage currents. DR is calculated as:

$$DR = \frac{E_{10} - E_{11}}{\Delta t} \qquad \text{volts/second}$$

where E_{10} and E_{11} are the error voltage measurements made at times t_1 and t_2 and $\Delta t = (t_2 - t_1)$.

3.10 Power Supply Rejection Ratio (PSRR). The test circuit for PSRR is configured in the same manner as the input offset voltage test described in section 3.2. The measured output voltage E_{12} is made under nominal power supply conditions. The power supply to be tested is then changed by a predetermined amount (obtained from the procurement document), and the new output voltage E_{13} is then measured. PSRR is then calculated as:

$$PSRR = \frac{\Delta E_0}{100 * \Delta V_{CC}}$$

where: ΔE_0 = Change in output voltage ($E_{13} - E_{12}$)
ΔV_{CC} = Change in supply voltage

This measurement is then repeated for all other device power supplies.

3.11 Power Supply Current (ICC). Power supply current for all device power supplies shall be measured using method 3005.1 of MIL-STD-883C. This includes positive and negative bias supplies (+VCC, -VCC), as well as any logic voltage supply.

3.12 Input Leakage Currents (IIH, IIL). Leakage currents at the logic input(s) of the S/H amplifier will be measured using methods 3010.1 (IIH) and 3009.1 (IIL) of MIL-STD-883C.

3.13 Acquisition Time (t_{aq}). An iterative procedure is used to measure t_{aq}. With the S/H amplifier in the hold state, the signal input is stepped from 0 to +FS volts. After a delay of approximately 100 µs, a sample pulse of duration equal to at least 10 times the specified t_{aq} is applied to the control input. The difference between the input and test device output is monitored at the output of the error amplifier. Repeat this cycle reducing the sample mode pulse width until there is an 0.01% change in the error amplifier output from the initial value measured. The sample pulse width for this condition is the acquisition time. Figure 2 shows an automatic flow chart for this procedure.

3.14 Aperture Time (t_{ap}). An iterative procedure is used to measure t_{ap}. The control input is stepped from sample to hold level with the signal input at 0 volts. After a delay equal to ten times the specified aperture time, the input signal is stepped to +FS volts, held at that level for a period longer than the acquisition time and then returned to 0 volts. The output at the error amplifier is measured and recorded. The cycle is repeated with decreasing delay times between the logic signal step and the input signal step. The delay time for which the error amplifier output changes by 0.01% from its initial value is the aperture time. The procedure is repeated for all combinations of transitions between 0 and +FS volts and 0 and -FS volts. Figure 3 shows an automatic flow chart for this procedure.

3.15 Transient Response (TR_{ts}, TR_{os}). Transient response time and transient response overshoot are measured in the circuit of figure 4 with the amplifier in the sample mode. An input pulse of rise time 50 ns and amplitude 100 mV is applied at the analog input of the amplifier and the output is observed on the oscilloscope. The measurements are made for both common mode input limit voltages, for example, if nominal values of +VCC and -VCC are +15 V and -15 V and the common mode range is ±11.5 V, the values of ±VCC will be +3.5 V and -26.5 V for the higher limit and +26.5 V and -3.5 V for the lower limit.

3.16 Noise Voltage. Noise voltage is measured as an rms voltage at the output of a filter as shown in the circuit of figure 5. The amplifier is placed in a sample mode to produce $en_{(S)}$ and in a hold mode to produce $en_{(H)}$. Input resistors and logic control voltages will be defined in the detail specifications.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document.

a. Hold capacitor capacitance.
b. Positive and negative bias voltages and logic voltage for each test ($+V_{CC}$, $-V_{CC}$, V_{Logic}).
c. Input signal voltage (V_{IN}) forced for each test.
d. Negative and positive voltage values to be appied for $V_{IO}(adj)$ test
e. Time delay for V_{HS} measurement.
f. Measurement times for DR(+) and DR(-) tests.
g. ΔVCC for PSRR tests.
h. Resistors and input voltage levels required for noise voltage test.
i. Temperatures T_1 and T_2 for input offset drift test.
j. Limit values for each parameter tested.
k. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.

PARAMETER	NOTES	INPUT VOLTAGE	S/H LOGIC	ACTUATED RELAYS	MEASUREMENT PIN	MEASUREMENT VALUE	EQUATION	UNITS
V_{CAL}	1	---	---	K_4	E_{OUT}	E_1	$V_{CAL} = E_1/100$ (NON-INVERTING) $V_{CAL} = E_1/100$ (INVERTING)	Volts
V_{IO}	2	0	S		E_{OUT}	E_2	$V_{IO} = E_2/100 - V_{CAL}$	Volts
I_{IB}	2	0	S	K_2	E_{OUT}	E_3	$I_{IB} = \frac{E_2 - E_3}{100,000}$	Amperes
V_{HS}	3,4	V_{IN}	S H	K_1	E_{OUT} E_{OUT}	E_4 E_5	$V_{HS} = \frac{E_5 - E_4}{100}$	Volts
A_E		10 V -10 V	S S	K_1	E_{OUT} E_{OUT}	E_6 E_7	$A_E = \frac{E_6 - E_7}{20}$	%
F_{RR}		V_{IN} $V + \Delta V_{IN}$	H H	K_1	E_{OUT} E_{OUT}	E_8 E_9	$FRR = 20*\log\left(\frac{100\Delta V_{in}}{E_9 - E_8}\right)$	db
DR	5	V_{IN}	S H	K_1	E_{OUT} E_{OUT}	E_{10} E_{11}	$V_{HS} = \frac{E_{10} - E_{11}}{100}$	Volts
t_{aq}	6	V_{IN}	S/H pulsed	K_1	E_{OUT}	t_1	$t_{aq} = t_1$	Seconds
t_{ap}	7	V_{IN}	S/H pulsed	K_1	E_{OUT}	t_2	$t_{ap} = t_2$	Seconds
$TR_{(ts)}$	8	V_{IN} (pulse)	S		E_{OUT}	---	$TR_{(ts)} = \Delta t$	Seconds

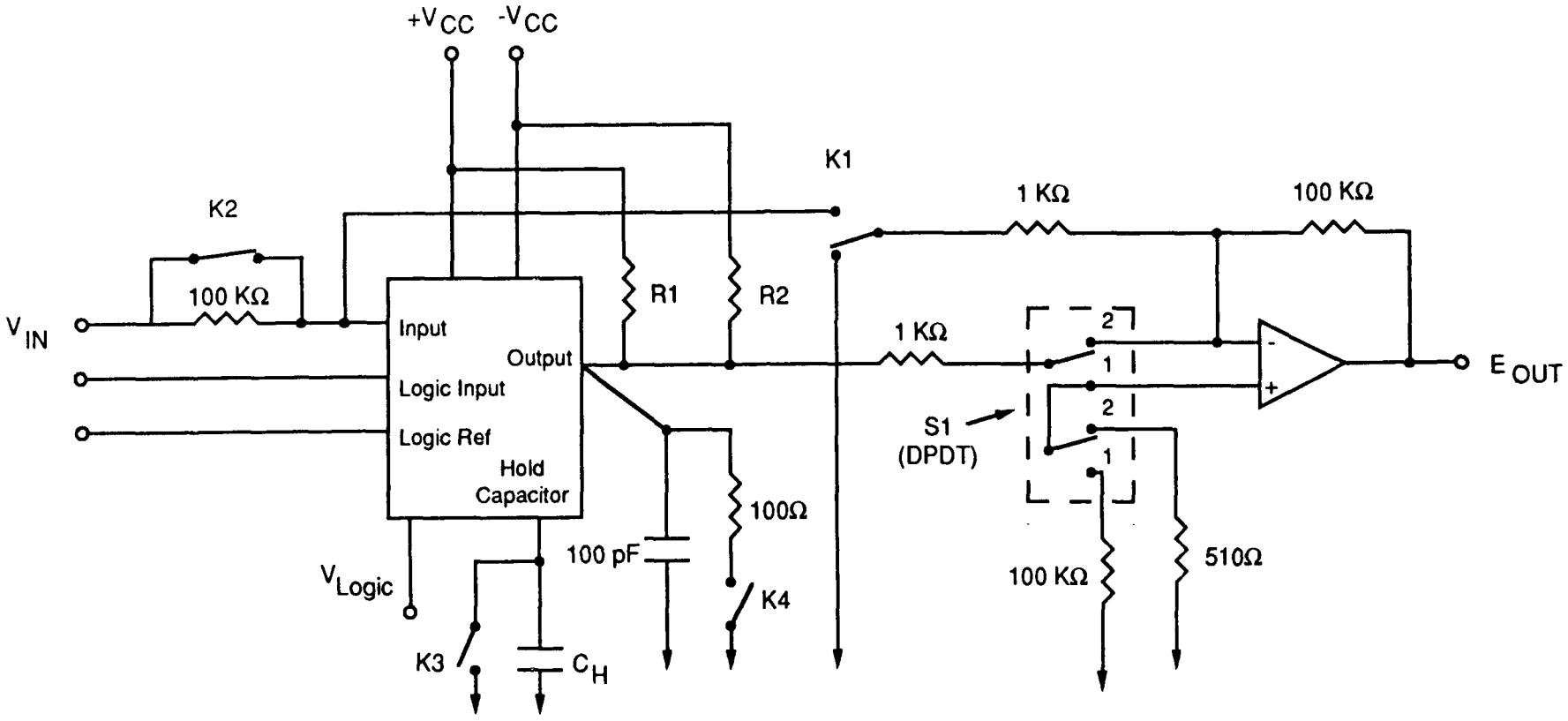
Table 1. Sample-and-Hold Amplifier Tests

PARAMETER	NOTES	INPUT VOLTAGE	S/H LOGIC	ACTUATED RELAYS	MEASUREMENT PIN	MEASUREMENT VALUE	EQUATION	UNITS
$TR_{(os)}$	8	V_{IN} (pulse)	S		E_{OUT}	---	$TR_{(os)} = \Delta V_o / V_o$	Volts
PSRR	9	0 0	S S		E_{OUT} E_{OUT}	E_{12} E_{13}	$PSRR = 20*\log\left(\frac{100\Delta V}{E_{12} - E_{13}}\right)$	db
N_O	10 10	V_{IN} V_{IN}	S H		E_{OUT} E_{OUT}	E_{14} E_{15}	$N_O(s) = E_{14}$ $N_O(h) = E_{15}$	V_{rms} V_{rms}

Notes

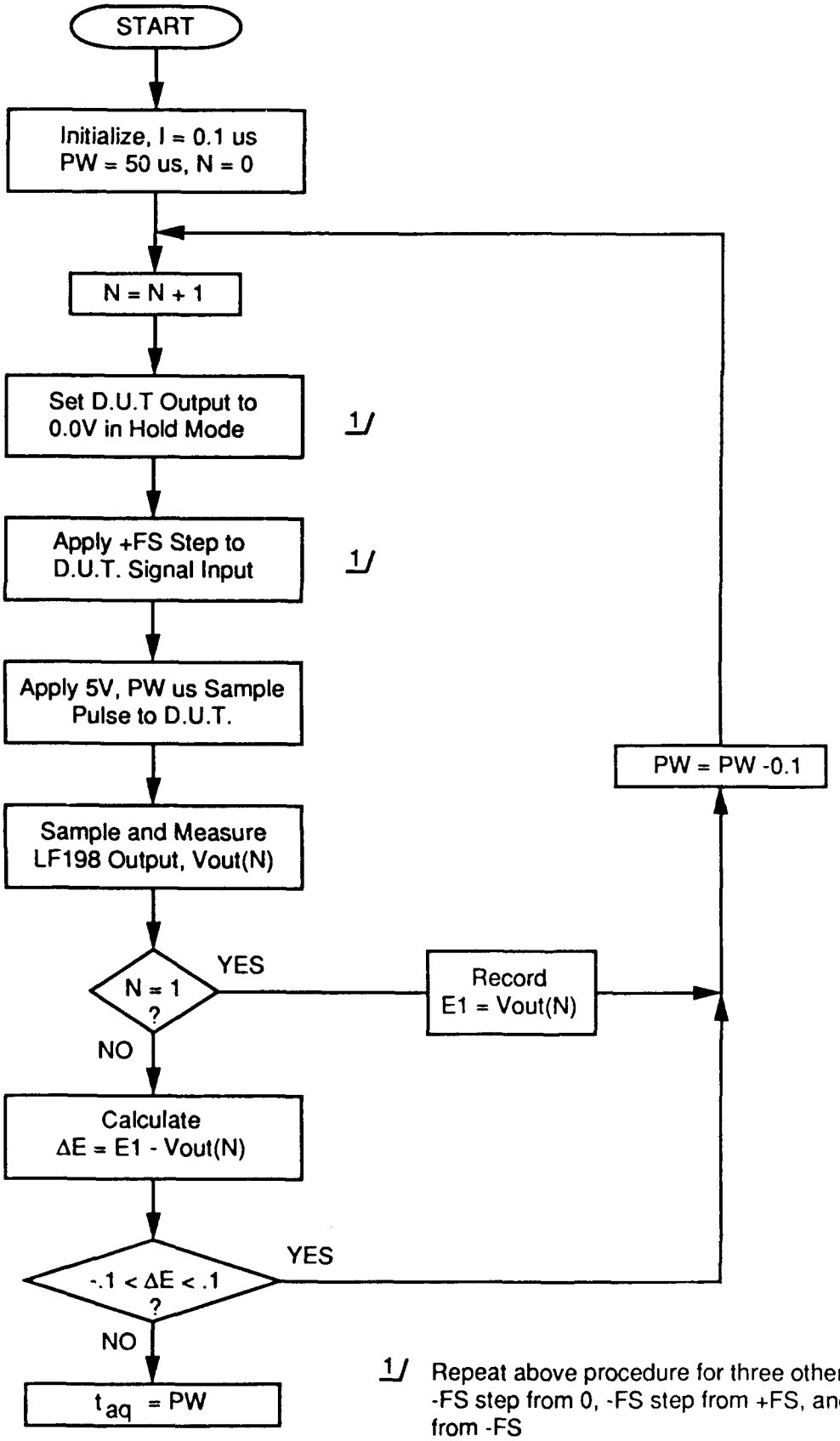
1. Measured with test device removed from socket.
2. For V_{IN} other than 0 volts, common mode conditions can be exercised by grounding the input and swinging the power supplies to their nominal level minus the common mode voltage.
3. Logic input steps should have a rise time of 5ns or less.
4 Hold measurement should be made within 50 us of the hold command, especially at 125°C.
5. Droop ios measured over a 100 ms interval starting within 100 μs of the hold command.
6. See Section 3.6 and figure 2.
7. See Section 3.7 and figure 3.
8. See circuits and waveforms in figure 4.
9. E_{12} is measured at $+V_{CC}(max)$ and $-V_{CC}(min)$, for +PSRR, E_{13} is measured at $+V_{CC}(max) - \Delta V$ and $-V_{CC}(min)$; for -PSRR E_{13} is measured at $+V_{CC}(max)$ and $-V_{CC}(min) + \Delta V$ where ΔV is a specified value.
10. See circuit in figure 5.

Table 1. Sample-and-Hold Amplifier Tests (cont)



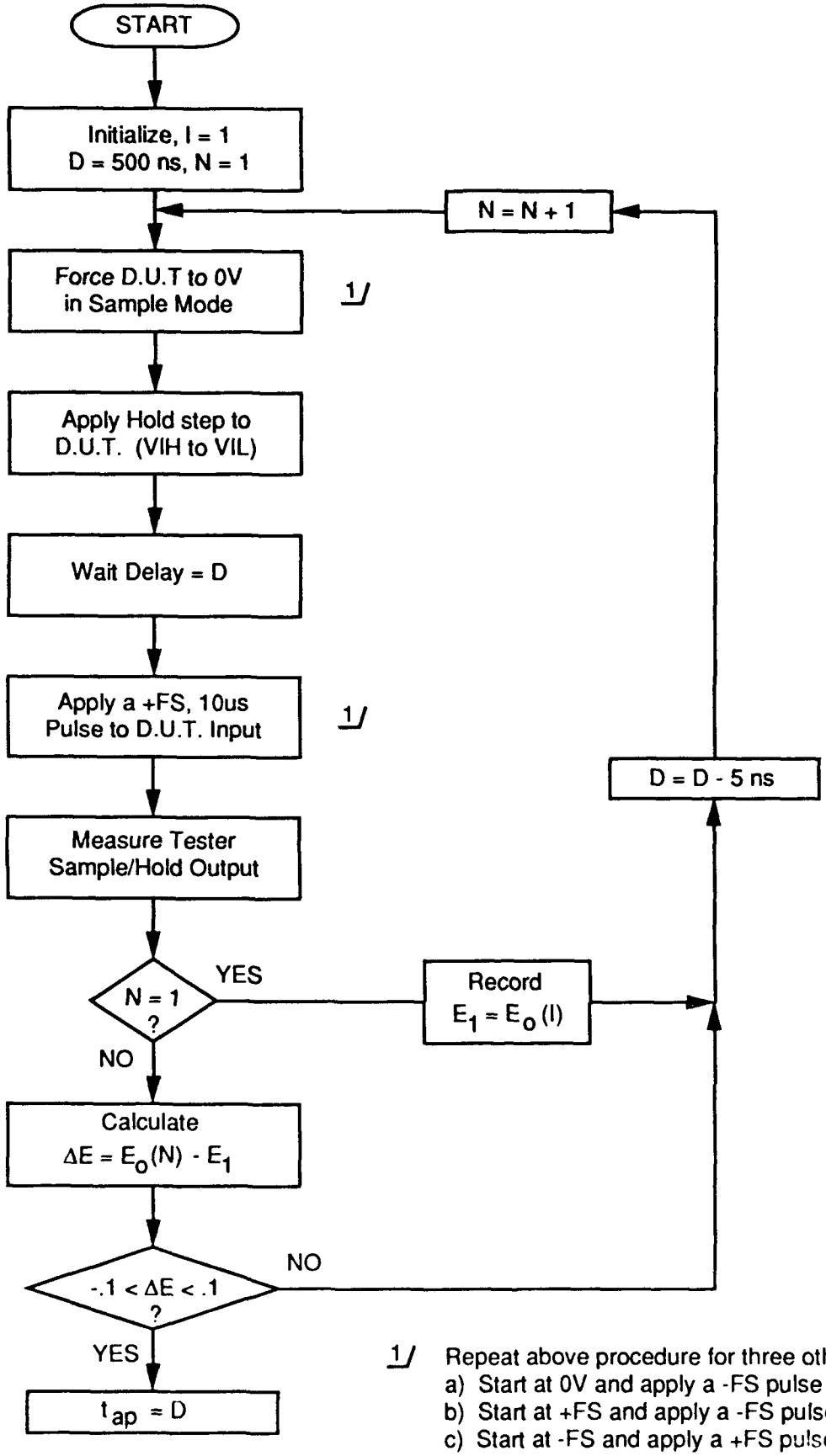
Notes: 1. All Resistors +/- .1%
2. S1 shown in position for inverting S/H

Figure 1. Test Circuit for Sample-and-Hold Amplifiers



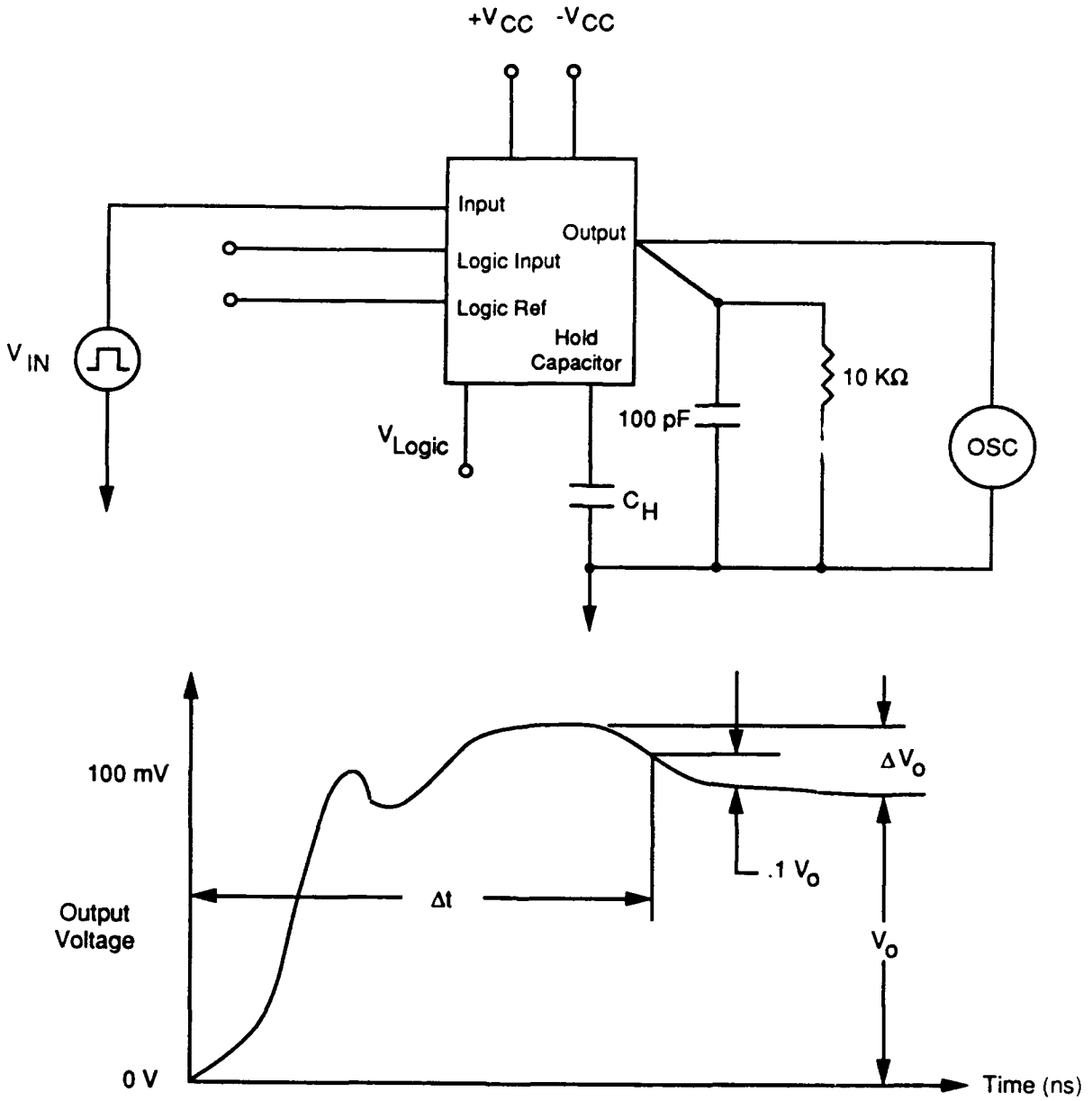
1/ Repeat above procedure for three other cases as follows: -FS step from 0, -FS step from +FS, and +FS step from -FS

Figure 2. Acquisition Time Flow Chart Example



1/ Repeat above procedure for three other cases as follows:
a) Start at 0V and apply a -FS pulse
b) Start at +FS and apply a -FS pulse
c) Start at -FS and apply a +FS pulse

Figure 3. Aperture Time Flow Chart Example



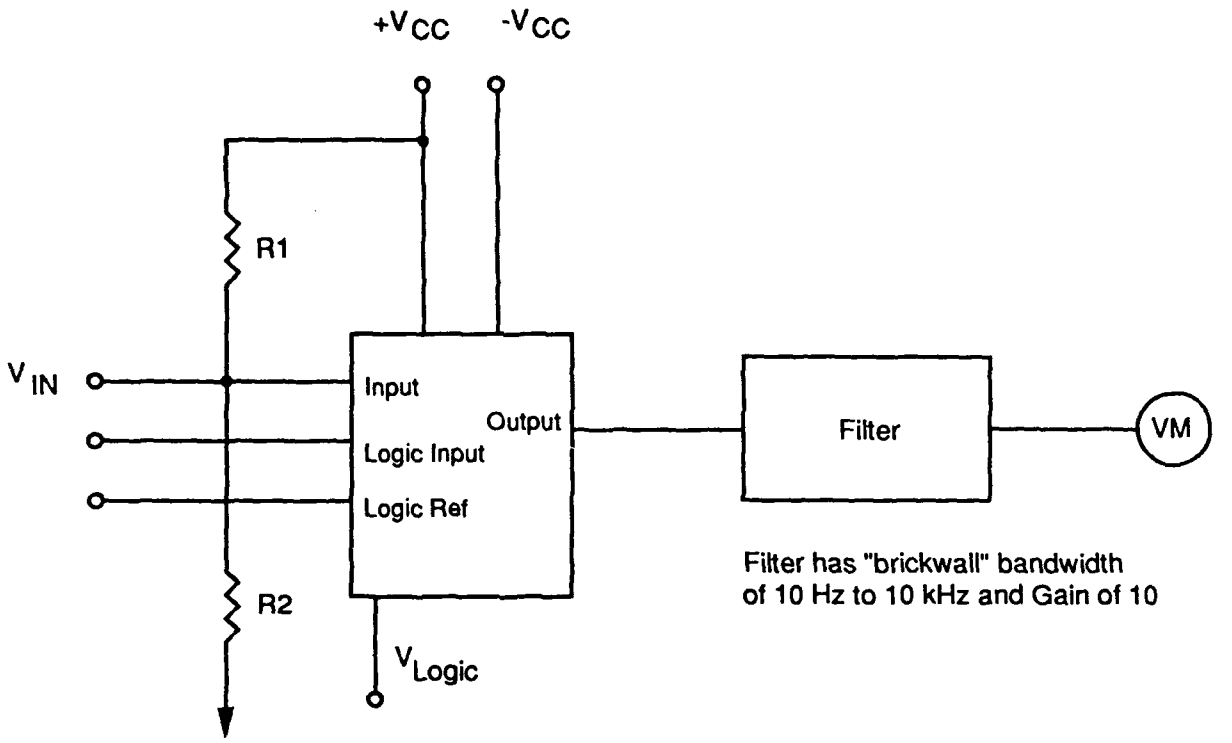
Transient Response Waveform

Equations: $TR_{(ts)} = \Delta t$

$TR_{(os)} = \Delta V_o / V_o$

Notes:
1. +VCC and -VCC shall be at common mode limits
2. Any high frequency ringing shall be over within 1 μs
3. After its peak, the major loop response shall be without further oscillations
4. Input pulse shall have amplitude of 100 mV and rise time less than 50 ns

Figure 4. Transient Response Test Circuit and Waveforms



Note: $E_{OUT} \approx 0.1\,V_{rms}$

Figure 5. Noise Circuit For Sample-and-Hold Amplifiers

METHOD 4006

DIGITAL-TO-ANALOG CONVERTER PARAMETERS

1.0 PURPOSE. This method establishes the means for measuring gain error, unipolar offset voltage error, bipolar offset error, bipolar zero error, offset drift, integral linearity, differential linearity, power supply sensitivity ratio, output noise of a unipolar or bipolar, digital-to-analog converter (DAC), the full scale and zero scale current outputs of a current output DAC, and settling time for voltage output and current output digital-to-analog converters.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Resolution (N). The number of binary bits resolved as an analog voltage by the DAC.

1.1.2 Input Code (n). For the purposes of this specification n is defined to be the decimal equivalent of the binary input code to the DAC. The binary form of the number is denoted by the subscript B, i.e., n_B.

1.1.3 Reference Voltage (V_{REF}). An internal or externally provided voltage source that establishes the range of output analog voltages generated by the DAC.

1.1.4 Transfer Function. The input/output relationship of a DAC consistings of a set of discrete points corresponding to the number of digital codes for which each voltage is a fraction of the reference quantity.

1.1.5 Unipolar DAC. A DAC having outputs of one polarity (positive or negative) only. The transfer function for a unipolar DAC having a natural binary input code is given by:

$$V_o = V_{FS}^* \sum_{i=1}^{N} \left(\frac{b_i}{2^i} \right)$$

The coefficients, b_i, represent the logic levels of the input bits which may be either 1 or 0. N is the number of input bits.

1.1.6 Bipolar DAC. A DAC having both positive and negative polarity output. The transfer function for a bipolar DAC having a twos complement binary input code is given by:

$$V_o = -V_{FS} + 2V_{FS}^* \sum_{i=1}^{N} \left(\frac{b_i}{2^i} \right)$$

1.1.7 Voltage Range (VR). The range of output voltages produced from a digital input code of $n = 0_B$ to $n = (2^N-1)_B$. The most positive voltage is indicated by VR_{LO} and the most negative by VR_{HI}.

1.1.8 Least Significant Bit (LSB). The least significant bit of the DAC input code.

1.1.9 Least Significant Bit Voltage (V_{LSB}). The nominal change in the analog output of the DAC for a 1 LSB change in the input code.

$$V_{LSB} = \frac{VR_{HI} - VR_{LO}}{2^N}$$

1.1.10 End Points. The analog output voltages of the DAC corresponding to the highest and lowest input codes, i.e., all 1's and all 0's. In the case of a current output DAC, the end point voltage outputs are obtained by converting the output from current to voltage.

1.1.11 Error Voltage. The error voltage is the difference between the ideal analog output voltage for a specified digital input and the actual output voltage of the DAC at that input.

1.1.12 Gain Error (A_E). The difference between the actual and the ideal gain expressed as a percent of full-scale. Gain is measured between zero and full scale.

1.1.13 Gain Error Drift (dA_E/dT). The gain error is the difference in gain errors at 25 °C and the upper or lower temperature limit, usually 125 °C and -55 °C, divided by the temperature span.

1.1.14 Offset Voltage Error (V_{OS}). The analog voltage error at zero scale for a DAC operating in the unipolar mode.

1.1.15 Offset Drift ($\Delta V_{OS}/\Delta T$). Offset drift is the offset voltage change in LSB voltage per degree centigrade.

1.1.16 Bipolar Zero Error (V_{ZE}). For a bipolar DAC the mid scale binary input code will normally correspond to zero output voltage. The deviation of the output voltage from zero with the input code set to binary 10.....00 is defined to be the bipolar zero error.

1.1.17 Integral Linearity Error (ILE). The maximium deviation of the analog output from a straight line drawn between the end points, expressed in least significant bit (LSB) units.

1.1.18 Differential Linearity Error (DLE). The maximum deviation of an actual analog output step, between adjacent input codes, from the ideal step value of 1 LSB based on the gain of the particular DAC, that is, the full scale range divided by 2^N where N is the number of binary bits.

1.1.19 Full Scale Output Current (I_{FS}). The output current from a current output DAC when the maximium digital input is applied.

1.1.20 Zero Scale Output Current (I_{ZS}). The output current from a current output DAC when the minimum digital input code is applied.

1.1.21 Power Supply Sensitivity Ratio (PSSR). The power supply sensitivity ratio is the change in full scale analog output voltage of the DAC caused by a deviation of a power supply voltage from the specified level. The change is measured as LSB units per percent change in power supply voltage.

1.1.22 Settling Time (t_{shl}, t_{slh}). The time required for the output of a DAC to approach a final value within the limits of a defined error band, for a step change in input. The settling times for a transition from high-to-low level output transition (t_{shl}) and for a low-to- high level output transition (t_{slh}) may be different.

1.1.23 Output Noise Voltage (N_o). The output noise from the DAC within a defined bandwidth and with a defined digital input word.

2.0 APPARATUS. The apparatus shall consist of a precision voltmeter, adjustable power supplies, a reference DAC which should have at least four bits greater resolution than the device under test, operational amplifiers and associated passive components and suitable switches to implement the test circuits of figures 1, 2 and 4.

2.1 DC voltmeter. The accuracy of the dc voltmeter will depend on the method used to perform static tests on the DAC. If the voltage output of the DAC is measured directly, the voltmeter shall have ten times or better accuracy than 1 lsb of the DAC configured for voltage output operation. If the reference DAC method is used, the dc voltmeter will have an accuracy to within 0.1% of the measured voltage corresponding to 1 LSB of the DAC in test as measured at the output of the error amplifier.

2.2 Reference Voltage Source. The reference voltage source shall have an accuracy equivalent to a DAC having N+4 bits of resolution where N is the resolution of the DAC in test. For example, 18 bits of resolution would be required in the reference voltage source to test a 14 bit DAC.

2.3 Programmable Reference Voltage Source. The programmable reference voltage source will be digitally programmable to an increment equivalent to 1 LSB of the converter under test. The accuracy of the reference voltage source shall be within 1/16 LSB of the DAC under test. For example if a 12-bit DAC is to be tested with a unipolar output voltage range of 10 volts, the reference voltage source shall be accurate to 153 microvolts.

2.4 Resistor Networks. Resistors in gain setting networks shall be accurate to within 0.1% over the required temperature range.

2.5 Pulse Generator. The pulse generator used in the settling time circuit shown in figure 2 shall be capable of providing a pulse of five volts amplitude from logic ground at a 1 kHZ frequency and 50% duty cycle.

2.6 Power Supplies. The device power supplies will be capable of providing bias and logic supply voltages required by the device specification.

2.7 Operational Amplifiers. The operational amplifier for the settling time circuit (figure 2) and noise test circuit (figure 4) should be a high-speed type with a bandwidth at least equal to one half the reciprocal of the settling time in MHZ.

2.8 Passive Components. Resistor and capacitor values are as indicated on all test figures. Resistors may be 5% tolerance (except those used in the resistor networks mentioned in section 2.4) and capacitors 10% unless otherwise specified.

2.9 Oscilloscope. Bandwidth of the oscilloscope should be 100 MHz minimum for settling times of 50 to 100 nanoseconds.

2.10 RMS Voltmeter. Bandwidth of the AC voltmeter used in the noise test circuit should be 10HZ to 100KHZ with 1 μv sensitivity.

3.0 PROCEDURE. Figure 1 shows the generic test configuration for the static tests. The figure and procedure are applicable to test both unipolar and bipolar DAC configurations. The method employed for the measurements is the reference voltage method. The operational amplifier, U2, amplifies the difference between the voltage output of the device under test and the programmable reference voltage by a factor of 100. The operational amplifier U1 converts the output of current output digital-to-analog converters to a voltage output and may be omitted in the test of voltage output DACs. Stabilizing networks, power supply decoupling and calibration components required for the practical implementation of the circuit are not shown. Table 1 shows the digital logic inputs and reference voltage for each measurement made and the equation for calculating the parameter. The digital inputs shown assume a positive logic device, binary ones and zeros are inverted in the case of complimentary logic device.

Figure 2(a) shows the generic test circuit for current output DAC settling time test and figure 2(b) shows the circuit for voltage output DAC settling time test. In both circuits the input of the DAC is pulsed from all ones to all zeros and the resulting output wave form, buffered by the operational amplilfier, is displayed on the oscilloscope. Schottky diodes in the feedback path of the preamplifier prevent saturation of the amplifier and limit the trace amplitude on the oscilloscope. The input and output waveforms are illustrated in figure 3. Figure 4 shows the test circuit for output noise. Amplifier U1 of this figure is omitted for voltage output DACs.

3.1 Output Offset Voltage (V_{OS}). To measure the output offset voltage the input code to the DAC is set equal to zero and the programmable reference voltage supply is set to the nominal output voltage for zero input code. For a converter in the unipolar mode this will be zero volts and for a converter in the bipolar mode this will be the most negative voltage in the nominal voltage range. The measured voltage at Terminal 1 is divided by 100 to obtain the voltage at the output of the DAC and this value is converted to LSB units by dividing by the nominal LSB voltage as defined in section 1.1.9.

3.2 Offset Drift ($\Delta V_{OS}/\Delta T$). Two values of offset drift are obtained by measuring the offset voltages at -55°C and at 125°C. For each measurement, the

difference from the offset voltage at 25°C is divided by the temperature difference and LSB voltage to obtain the offset voltage drift in LSBs per degree centigrade.

3.3 Gain Error (A_E). The gain error is obtained by measuring the error voltages at all zeros digital input and then at all ones digital input. The reference voltage for the error voltage measurement at all zeros is set equal to the lower limit of the nominal voltage range and at all ones to the upper limit of the nominal voltage range less a voltage equivalent to one binary bit (V_{LSB}). The all ones output is subracted from the all zeros output and the result divided by the nominal range for the DAC, (VR_{HI} - VR_{LO}). This result, expressed as a percentage of the nominal voltage output range, is the gain error of the DAC. The error amplifier gain factor and the percent multiplier of 100 cancel out in the computation.

3.4 Gain Error Drift (dA_E/dT). Two values for gain error are obtained by measuring the gain error at 25°C, -55°C and 125°C. The gain errors are calculated by taking the difference between gain errors at 25°C and each temperature limit and dividing by the temperature span.

3.5 Integral Linearity Error (ILE). Linearity error is measured by the end-point method. In this method, the integral linearity error is defined as the difference between the actual voltage output at a given binary input and voltage at that binary value for a straight line drawn between the actual voltage outputs at all zeros and all ones binary inputs. Since the generic test circuit measures the voltage deviation between the converter output and the programmed reference voltage, the computation must adjust for the offset voltage and gain error of the converter. The incremental gain error for each binary increment is calculated as S shown in Table 1. V_{IDEAL}, the difference between the programmed reference voltage and the ideal straight line voltage output of the converter is then calculated allowing for the offset voltage. The integral linearity error for binary input of value n is the difference between this value and the measured error voltage output at that point expressed in units of LSB.

3.6 Differential Linearity Error (DLE). The differential linearity error is obtained by measuring the error voltage output at two adjacent binary input codes and subtracting the lower code value from the higher. The result is expressed in LSB units. A value more negative than -1 LSB indicates that the converter is non-monotonic.

3.7 Full Scale Output Current (I_{FS}). The full scale output current of a current output digital-to-analog converter can be obtained by measuring the voltage at Terminal 2 of the test circuit with a full scale input code applied to the DAC. The current to voltage converter circuit, U_1 and R_4, must be calibrated to provide an accuracy in the current measurement within 0.1% of full scale current.

3.8 Zero Scale Current (I_{ZS}). The zero scale output current is measured at Terminal 2 with an input code of zero applied to the DAC.

3.9 Power Supply Sensitivity Ratio (PSSR). The power supply sensitivity ratio is obtained by measuring the change in the error voltage measured at full

scale corresponding to a specified change in a power supply voltage from nominal operating voltage. Only one power supply may be varied while making this measurement.

3.10 Power Supply Current (I_{CC}). Power supply current shall be measured for all device power supplies using the procedure outlined in method 3005.1 of MIL-STD-883C. For each test, the digital input code fed into the DAC while the measurement is made shall be specified in the procurement document.

3.11 Input Current (I_{IH}, I_{IL}). Input leakage currents shall be measured for all digital inputs on the DAC. I_{IH} shall be measured as outlined in method 3010.1 of MIL-STD-883C. I_{IL} shall be measured using method 3009.1.

3.12 Settling Time (t_{shl}, t_{slh}). With reference to figures 2(a), 2(b), and 3, the procedure for performing the settling time test is as follows:

1. With S_1 closed to V_{IN} and V_{IN} set to its final value, the coarse and fine adjustments are used to center the oscilloscope trace on the center of the horizontal graticule.

2. With S_1 closed to ground, the oscilloscope gain is adjusted for a vertical gain of 1/2 least significant bit (LSB) per cm.

3. With S_1 closed to V_{IN}, a logic pulse is applied to V_{IN} and the output waveform is observed to obtain t_{shl} and t_{slh}.

3.13 Internal Reference Voltage (V_{REF}). Where an internal reference voltage is available, it can be measured directly with a precision voltmeter as indicated figure 1.

3.14 Output Noise Voltage (N_o). Using the noise test circuit of figure 4, the inputs to the DAC under test are set to high states. The output noise of the DAC is then measured with an rms voltmeter with a bandwidth of 10 HZ to 100KHZ. Output noise is then measured with all inputs low. Noise output from the voltage reference is also measured. Noise output for the device is given by the following expression:

$$N_o = \frac{\sqrt{(N_o)^2 \text{ for all bits on} - (N_o)^2 \text{ for all bits off} - (N_o)^2 \text{ for } V_{REF}}}{\text{Amplifier gain}}$$

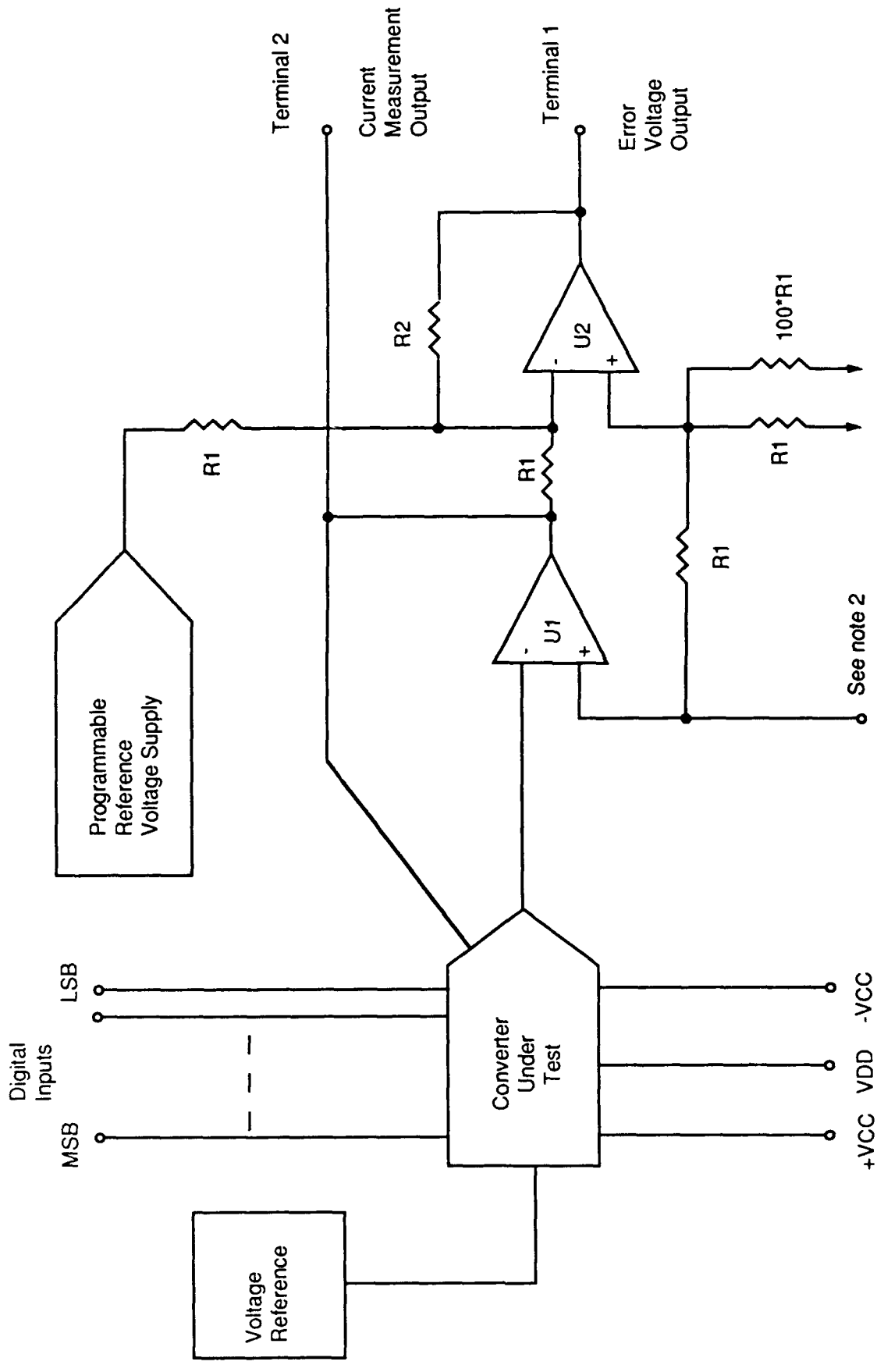
4.0 SUMMARY. The following details shall be specified in the applicable procurement document for specified values of R1, R2 and R3.

a. Type of DAC, voltage or current output.
b. Resistor and Capacitor values for each test circuit.
c. All power supply levels for each test.
d. Forcing voltages for I_{IH} and I_{IL}.
e. Limit values for each parameter tested.
f. Noise amplifier gain
g. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.

Symbol	Digital Input	Reference Voltage	Value	Meas. Term.	Equation	Units
V_{OS}	0 ---> 0_B	VR_{LO}	E_1	1	$V_{LSB} = (VR_{HI}-VR_{LO})/2^N$ $V_{OS} = \frac{E_1}{100(V_{LSB})}$	LSB
A_E	0 ---> 0_B 1 ---> 1_B	VR_{LO} $VR_{HI}-V_{LSB}$	E_1 E_N	1 1	$A_E = \frac{E_1 - E_N}{(VR_{HI} - VR_{LO})}$	%FS
ILE_n	n_B	$VR_{LO}+2^nV_{LSB}$	E_n	1	$S = \frac{E_N - E_1}{2^N - 1}$ $V_{IDEAL} = nS - E_1$ $ILE_n = \frac{E_n - V_{IDEAL}}{100(V_{LSB})}$	LSB
DLE	n_B $(n+1)_B$	$VR_{LO}+2^nV_{LSB}$ $VR_{LO}+2^{n+1}V_{LSB}$	E_n E_{n+1}	1	$DLE = \frac{(E_{n+1} - E_n)}{100(V_{LSB})}$	LSB
I_{FS}	1 ---> 1_B	----	EI_1	2	$I_{FS} = \frac{EI_1}{R4}$	Amps
I_{ZS}	0 ---> 0_B	----	EI_2	2	$I_{ZS} = \frac{EI_2}{R4}$	Amps
PSSR[1]	0 ---> 0_B	----	E_R	1	$PSSR = \frac{(E_1 - E_R)}{100(V_{LSB})(\Delta Vps)}$	$\frac{LSB}{V}$

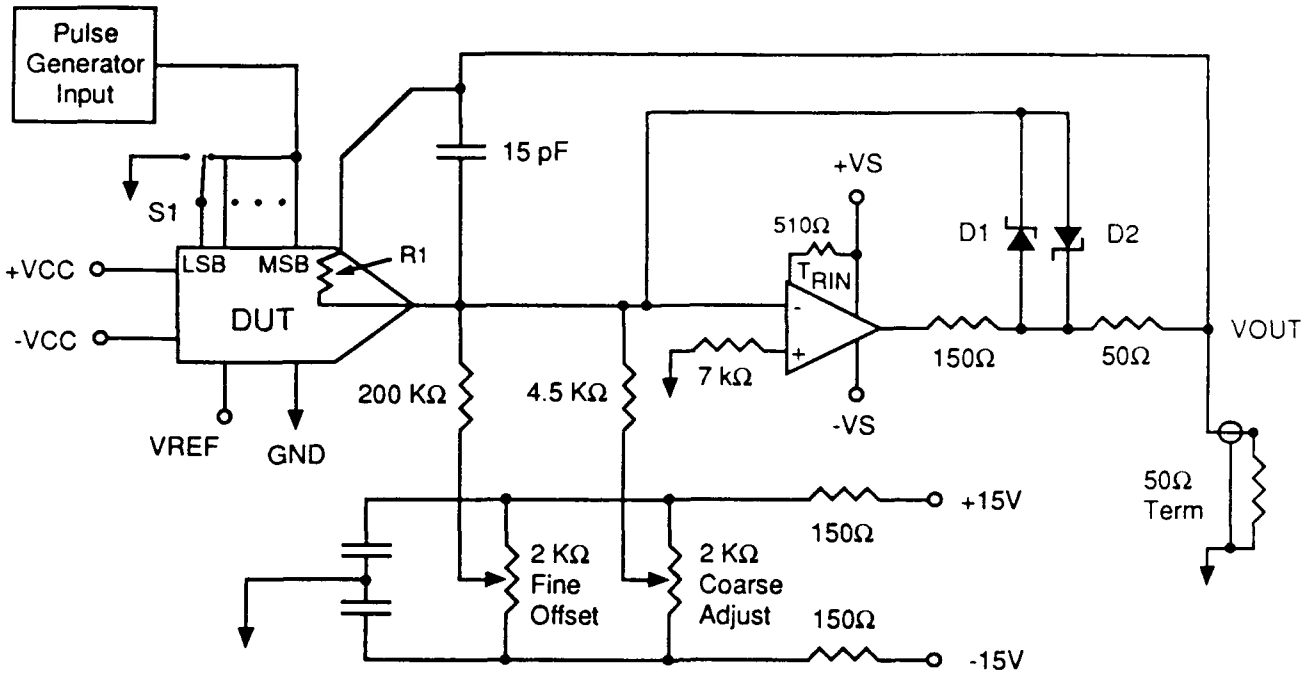
Notes: [1] Power supply voltage is incremented or decremented by ΔVps from the nominal level.

Table 1. Equations For D/A Converter Static Parameters

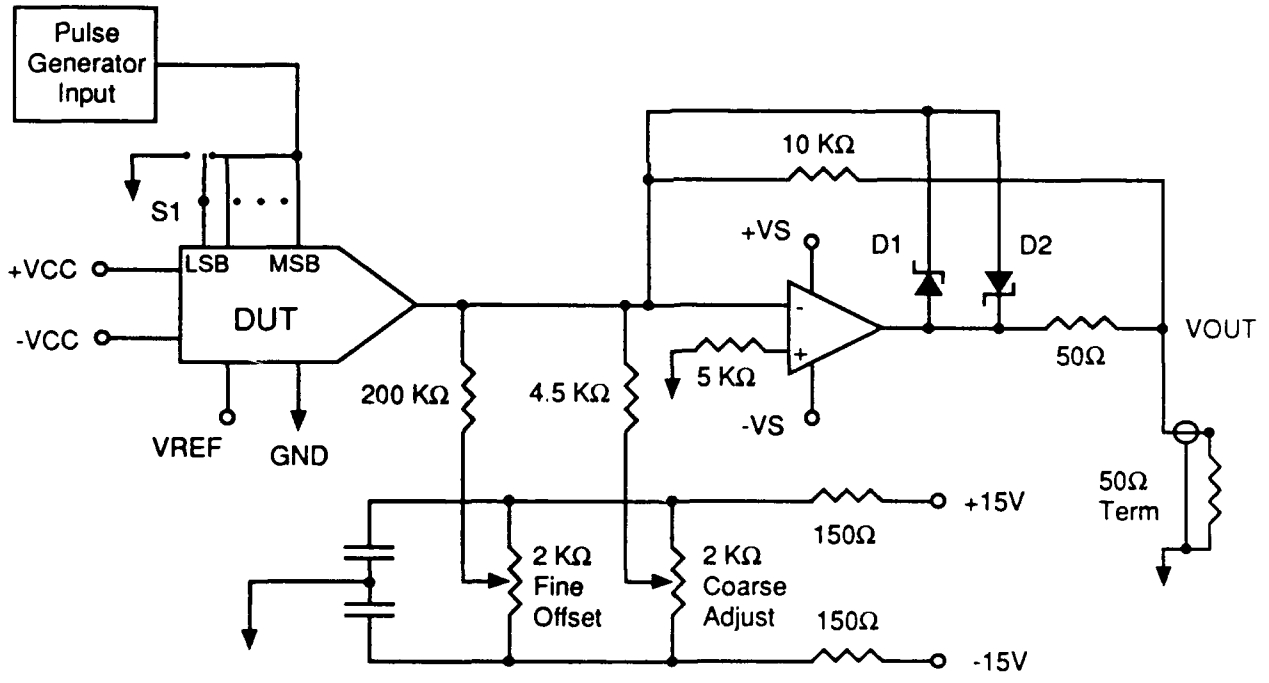


Note: 1. R2 = 100*R1
2. Compliance voltage terminal

Figure 1. DAC Static Test Circuit



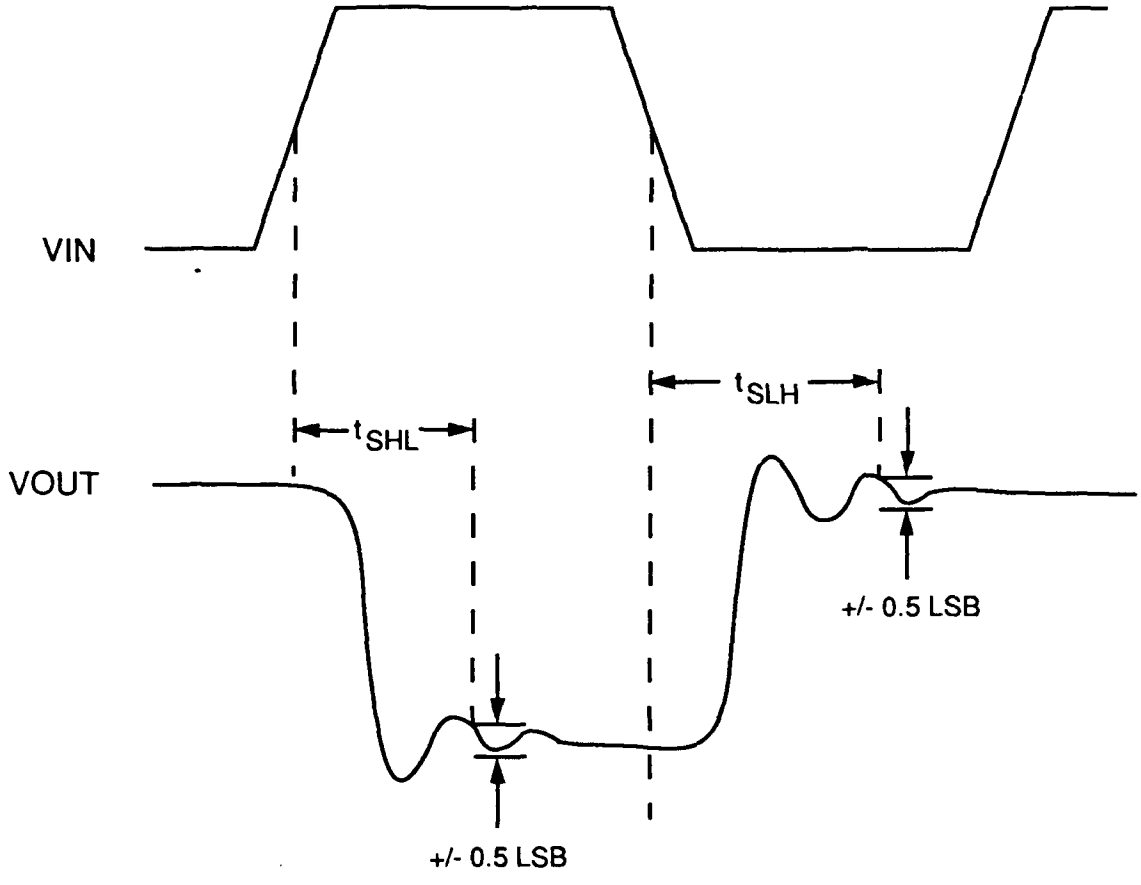
(a) Test Circuit For Current Output DAC



(b) Test Circuit For Voltage Output DAC

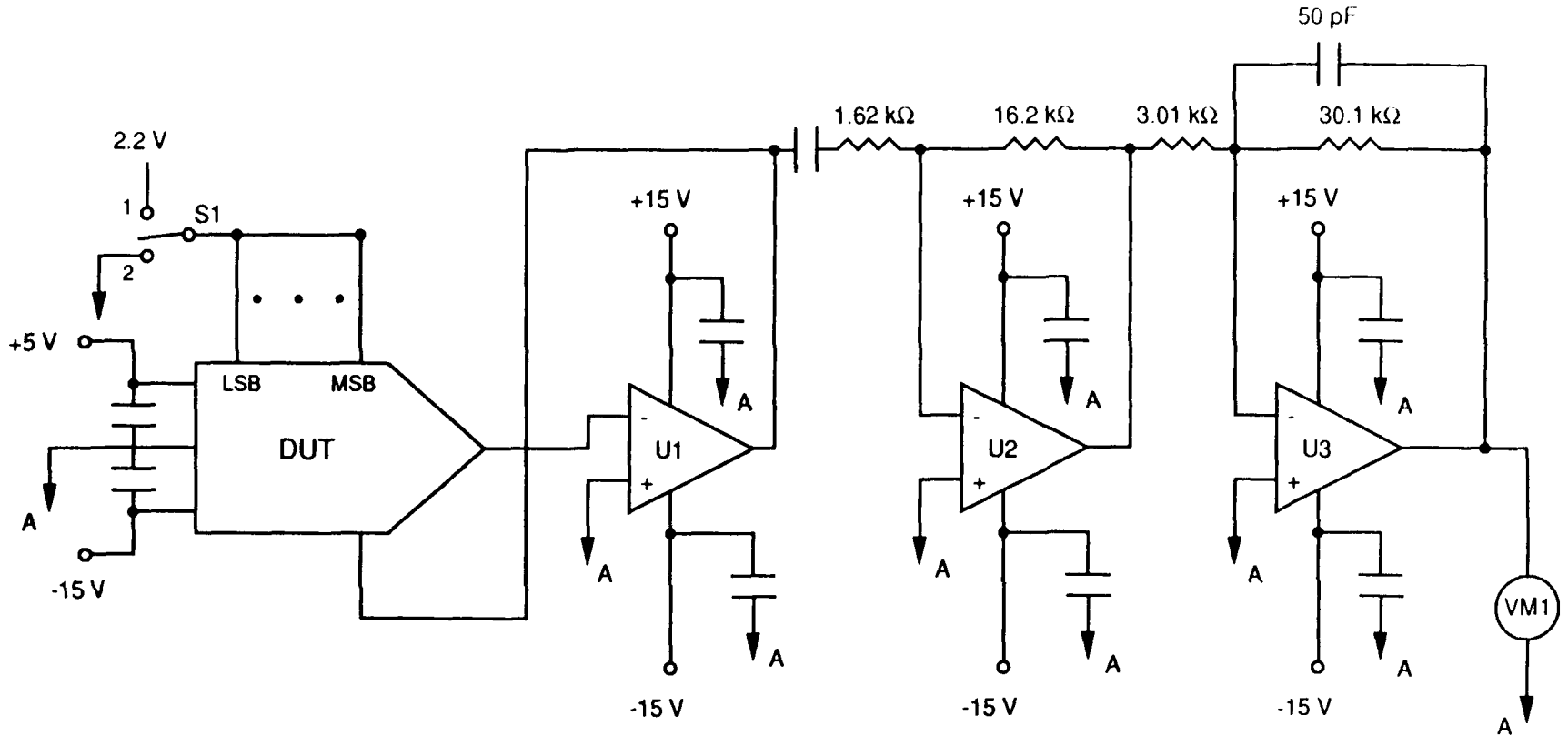
Notes:
1. De-coupling capacitors are required for +VCC, -VCC, +VS, and -VS
2. Unless otherwise defined, all capacitors are 47 uF tantalum paralleled with 0.1 uF ceramic
3. D1 = D2 = MP 5082-2835 or equivalent
4. R1 is input feedback resistor

Figure 2. Settling Time Test Circuits



Note: Rise and Fall times of the input waveform (10% to 90%) are as specified in the procurement document.

Figure 3. Waveforms For Settling Time Measurement



Notes:
1. Unless otherwise specified, all capacitors are 47 uF tantalum paralleled with 0.1 uF ceramic
2. VM1 shall be true RMS reading with a bandwidth greater than 100 kHz
3. U1, U2, and U3 shall have a gain-bandwidth product greater than 5 MHz and input noise density less than 10 nV/$\sqrt{\text{Hz}}$
4. All "A" point ground connections shall return to single unipoint ground at DUT ground pin
5. With S1 in position 2, the measured RMS noise voltage shall be less than 1.0 mV rms (Noise for all bits off)
6. With S1 in position 1, the measured rms noise voltage shall be: N_o for DUT = $\sqrt{\frac{(N_o)^2 \text{ all bits on} - (N_o)^2 \text{ all bits off}}{100}}$
7. If the DUT contains an internal operational amplifier, U1 should be omitted from circuit

Figure 4. Test Circuit For Noise Tests

METHOD 4007

ANALOG-TO-DIGITAL CONVERTER PARAMETERS

1.0 PURPOSE. This method establishes the means for measuring gain error, offset voltage error, zero error, full-scale voltage error, integral linearity error, differential linearity error, power supply sensitivity ratio, transition uncertainty, power supply current, input and output currents, and output voltage of a unipolar or bipolar, analog-to-digital converter (ADC).

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Reference Voltage (V_{REF}). An internally or externally supplied voltage which establishes the full scale voltage range of the ADC.

1.1.2 Full Scale Voltages (V_{FS}). The maximium voltage inputs that can be resolved by the ADC. These voltages will be some multiple of the internal or external reference voltage supplied to the ADC.

1.1.3 Resolution (N). The number of binary output bits of an ADC.

1.1.4 Output Code. The binary code at the digital outputs of the ADC. In this specification the binary output code is denoted by n where n is the decimal equivalent of the binary output code. The subscript B is added to denote the binary form of the number, i.e., n_B.

1.1.5 Most Significant Bit (MSB). The highest order binary bit in the output code of the ADC.

1.1.6 Most Significant Bit Voltage (V_{MSB}). The value in volts of the the most significant bit resolved by the ADC. The ideal value of the MSB is:

$$V_{MSB} = \frac{V_{FS}}{2} \qquad \text{(volts)}$$

1.1.7 Least Significant Bit (LSB). The lowest order binary bit in the output code of the ADC.

1.1.8 Least Significant Bit Voltage (V_{LSB}). The value in volts of the least significant bit resolved by the ADC. The ideal value of an LSB is found by dividing the full scale voltage by the magnitude of the binary resolution of the ADC. The ideal value of 1 LSB is:

$$V_{LSB} = \frac{V_{FS}}{2^N} \qquad \text{(volts)}$$

1.1.9 Code Transition. A code transition for a given binary output code, n_B, of the ADC is the transition between the given output code and a binary output code 1 bit greater, i.e., between n_B and $(n+1)_B$.

1.1.10 Transition Voltage (V_{IN}). $V_{IN}(n)$ is the analog voltage at the input of the ADC at which a transition occurs at the ADC output between binary output code n_B and $(n+1)_B$.

1.1.11 Ideal Analog Input Voltage ($V_{IN}(ideal)$). This is the ideal analog input voltage at which a code transition will occur for a given binary output code.

1.1.12 Zero Voltage Error (Z_E, BZ_E). The unipolar zero voltage error (Z_E) and the bipolar zero voltage error (BZ_E) are the input offset voltages for zero output code transition.

1.1.13 Code Width Error (CWE). Code width error is the measured width of a 1 LSB step in volts minus the ideal width of 1 LSB step in volts.

1.1.14 Unipolar Offset Error (V_{IO}). The unipolar offset error is the difference between the actual value of the first transition voltage and the ideal 1 LSB voltage minus the code width error voltage.

$$V_{IO} = V_{IN}(0) - CWE - V_{IN}(ideal) \qquad \text{(volts)}$$

1.1.15 Gain Error (A_E, BA_E). Unipolar gain error (A_E) and bipolar gain error (BA_E) are the difference between the actual and the ideal analog output range, expressed as a percent of full-scale. It is the deviation in the slope of the ADC transfer characteristic from the ideal.

$$AE = \frac{(V_{IN}(2^N-2) - V_{IN}(0)) - (V_{FS} - 2V_{LSB})}{V_{FS} - 2V_{LSB}}$$

Where $V_{IN}(2^N-2)$ is the voltage of the transition to all 1's binary output.

1.1.16 Full Scale Voltage Error (V_{FSE}). The full scale voltage error is the difference between the measured voltage of the final transition and the ideal voltage for that transition. A bipolar ADC will have positive and negative full scale errors ($+V_{FSE}$, $-V_{FSE}$) while a unipolar ADC will have one or the other depending on whether the full scale analog input voltage is a negative or a positive voltage. The final transitions are those for output code 0_B and $(2^N-2)_B$ (all binary bits equal to 1 except the LSB). $V_{IN}(ideal)$ at the final transition will be one V_{LSB} in magnitude less than the full scale voltage defined above.

$$V_{FSE} = \frac{V_{IN}(2^N-2) - V_{IN}(ideal)}{V_{LSB}} \qquad \text{(LSB)}$$

where

$$|V_{IN}(ideal)| = |V_{FS}| - V_{LSB}$$

1.1.17 Integral Linearity Error (I_{LE}). Integral linearity error is defined as the deviation of the transfer function from an ideal straight line drawn through the end points of the transfer function. The initial end point is that for the transition from all zeros to the LSB equal to 1 (n = 0). For a

unipolar ADC the coordinates for that point on the transfer curve are Z_E, and output binary code 1_B (n = 0). The full scale end point coordinates are $V_{IN}(2^N-2)$ and output binary code $(2^N-2)_B$. The integral linearity error at the end points will be zero by definition and the I_{LE}s at intermediate points are obtained from the equation:

$$I_{LE} = \frac{V_{IN}(n) - V_{IN}(ideal)}{S} \quad \text{(LSB)}$$

where n is a binary transition between n = 1 and n = 2^N-3

$$S = \frac{V_{IN}(2^N-2) - V_{IN}(0)}{2^N - 2} \quad \text{(volts/LSB)}$$

$$V_{IN}(n)(ideal) = nS - Z_E \quad \text{(volts)}$$

1.1.18 Differential Linearity Error (D_{LE}). Differential linearity error is the deviation in code width from the value of 1 LSB. The value of the LSB in volts is calculated from the end point transitions and is equal to S defined above. The D_{LE} at binary output code n is:

$$D_{LE} = \frac{V_{IN}(n) - V_{IN}(n-1)}{S} \quad \text{(LSB)}$$

1.1.19 Transition Uncertainty (N_T). The transition uncertainty is defined as the range of analog input voltages at one end of which there is a 16% probability for the occurrence of a transition to the next higher code, and at the other end an 84% probability for the occurrence of a transition.

1.1.20 Power Supply Sensitivity Ratio (PSSR). The power supply sensitivity ratio is the change in transition voltage for a percentage change in power supply voltage. PSSR is measured at the first and last transitions (binary 0 and binary 2^N-2 output codes). PSSR is expressed as the change in the transition point in LSB units per percent change in the power supply voltage.

$$PSSR(n) = \frac{\Delta V_{IN}(n)/V_{LSB}}{(\Delta V_{PS}/V_{PS})*100} \quad \text{(volts/\%FS)}$$

where n = 0 or 2^N-2

V_{PS} = power supply voltage

ΔV_{PS} = change in power supply voltage

1.1.21 Conversion Time (T_C). Conversion time is the amount of time elapsed from the start-conversion control signal until the conversion complete signal occurs.

2.0 APPARATUS. The apparatus shall consist of two digitally programmable voltage sources, adjustable power supplies, a summing amplifier and successive approximation circuitry to implement the test circuit of figure 1.

2.1 Digitally Programmable Voltage Sources (DPVS). The main programmable voltage source will be digitally programmable over the input voltage range of the ADC in test to an accuracy equal to 1/16 LSB of the ADC in test. The dithering voltage source will have an accuracy equal to 1/2 LSB and will be programmable over the input voltage range of the ADC in test. For example, to test a 12-bit ADC with an input voltage range of 10 V, the main voltage source will have a range of 10 volts and will be accurate to 153 μv. The dithering voltage source will have an accuracy of 610 μv.

2.2 Successive Approximation Circuitry. The functional requirement of the successive approximation circuitry is to adjust the voltage supplies of figure 1 until the digital output of the A/D converter in test makes a transition to a selected value. The circuitry will include as a minimum a digital register to store the selected digital value, a digital comparator to compare the A/D output to the stored value, and a successive approximation register to adjust the dithering power supply until the summed voltages of the two supplies converge on the required analog input to the A/D converter. Some conversion logic may be included to generate the correct digital input to the main voltage source such that the contribution of this source to the analog input to the converter in test is equal to the nominal transition point input voltage.

2.3 Reference Voltage Source. The reference voltage source will be accurate to within 1/2 LSB of the ADC under test. For example if a 12-bit ADC is to be tested, and the reference voltage is specified to be 10 volts, the reference voltage source shall be accurate to 1.22 mV.

2.4 Summing Amplifier. The summing amplifier shall be a precision operational amplifier of type MIL-M-38510/135 or equivalent.

2.5 Resistor Networks. Resistors in gain setting networks shall be accurate to within 0.1% over the required temperature range.

3.0 PROCEDURE. The method used to measure analog-to-digital converter parameters employs a digital feedback loop as shown in the generic test circuit of figure 1. An external reference voltage source may be required to set the voltage range of the ADC in test. The analog input voltage to the ADC is generated by summing the outputs of the two digitally programmable voltage sources. The accuracy and resolution of the analog input voltage is determined by the accuracy of the main programmable voltage source, by the resolution of the dither voltage source, and by the divider ratio R_1/R. It will typically be 0.01 LSB of the ADC in test.

The flow chart of Figure 2 describes the procedure for determining transition voltages for the ADC in test. Throughout this procedure, the search logic provides a signal to the ADC to initate repeated conversions. At the initiation of a measurement cycle, the dither voltage source is set to contribute zero incremental voltage and the main reference source is set to generate an analog input voltage to the ADC which results in the digital output code n_B. The adjustment of the main voltage source may require a preliminary search routine in which the voltage is adjusted above or below the nominal input voltage in increments of 1 V_{LSB} until the code n_B is detected at the digital output of the ADC. A binary search routine using the dither source is then performed. In this routine the dither voltage is adjusted upwards or downwards in diminishing increments until the transition from n_B to $(n+1)_B$ is located to the required resolution. As this search routine is performed, the transition will occur at each level of binary resolution of the dither source,

consequently, the dither voltage output must be decreased to reset the ADC to n_B prior to searching for the transition point at the next level of resolution. The transition points for the n_B to $(n+1)_B$ and the $(n+1)_B$ to n_B will generally be different and so the search logic must be capable of adjusting for this hysteresis.

The cycle described above is repeated at least ten times at each transition point. For all measured parameters defined above except N_T, the measured value of $V_{IN}(n)$ is defined as the average value at which there is an output code transition between n_B and $(n+1)_B$. For measurement of the transition uncertainty, N_T, two transition points are measured, that for which 16% of conversions are between n_B and $(n+1)_B$ and that for which 84% of the conversions are between n_B and $(n+1)_B$. The number of measurements required to make a statistical determination of the transition point will depend on the noise generated in the converter, occurring in the input signal or picked up in the test fixture wiring.

All test parameters are calculated from measured transition points. The measured transition voltage, E_N, in each case is the sum of the voltages from the main reference source and the dither voltage source adjusted for the ratios R/R and R_1/R. Table 1 summarizes the transition points measured and gives the equations for calculation of each parameter.

3.1 Zero Voltage Error (Z_E). The unipolar zero voltage error, Z_E, is obtained by measurement of the transition voltage from output code 0_B to 1_B as described in section 3.0. The measured value, E_0, is divided by the the LSB voltage defined in section 1.1.8 to obtain the result in LSB units.

$$Z_E = \frac{E_0}{V_{LSB}} \quad \text{LSB}$$

The result may be a positive or negative voltage.

3.2 Bipolar Zero Voltage Error (BZ_E). The bipolar zero voltage error, BZ_E, is obtained by measurement of the transition voltage at the midrange output code, $(2^{N-1} - 1)_B$. The result is expressed in LSB units.

$$BZ_E = \frac{E_{(2^{N-1}-1)}}{V_{LSB}} \quad \text{LSB}$$

3.3 Positive Full Scale Voltage Error ($+V_{FSE}$). Positive full scale voltage error applies to both unipolar and bipolar ADCs. It is obtained from measurement of the transition voltage of the last binary bit transition to all ones output from the ADC.

$$+V_{FSE} = \frac{E_{(2^N-2)} - V_{IN}(ideal)}{V_{LSB}} \quad \text{LSB}$$

where $V_{IN}(ideal) = V_{FS} - 2(V_{LSB})$

3.4 Negative Full Scale Voltage Error ($-V_{FSE}$). Negative full scale voltage error applies to bipolar ADCs. It is obtained from measurement of the transition voltage of the transition of all zeros to binary 1.

$$-V_{FSE} = \frac{E_0 - V_{IN(ideal)}}{V_{LSB}} \quad \text{LSB}$$

$$\text{where } V_{IN(ideal)} = (-V_{FS}) + V_{LSB}$$

3.5 Code Width Error (CWE). CWE can be obtained by measuring the transition points between successive 1 bit transitions. The difference between the two points is compared with the ideal V_{LSB}.

$$CWE = (E_2 - E_1) - V_{LSB}$$

where E_2 and E_1 are the measured transition points for outputs $n = 1_B$ and $n = 2_B$ from the ADC.

If so specified in the procurement document the code width can be measured over a span greater than one bit and divided by the binary width of the span. For example, the transition points for $n = 0_B$ and $n = 14_B$ may be measured and the difference in the measurements, $E_{14} - E_0$ divided by 14 to find CWE.

3.6 Unipolar Offset Error (V_{IO}). The unipolar offset error is obtained by measurement of the voltage for the transition to binary 1 from all zeros. Since this is the lowest binary transition but is, by definition, ideally equal to V_{LSB} rather than zero volts, the measurement is extrapolated to a hypothetical zero transition point by subtracting one LSB voltage. This must be the real voltage for 1 LSB which is obtained by subtracting the code width error from the ideal V_{LSB}:

$$V_{IO} = E_0 - V_{LSB} - CWE$$

3.7 Gain Error (A_E, BA_E). Gain error is obtained from measurements of the lowest and highest transition point voltages, $E_{(2^N-2)}$ and E_0. This procedure applies for both unipolar and bipolar gain error. The voltage difference between these two measurements is compared with the ideal difference and expressed as a percentage of the ideal difference. The full scale range (FSR) in this parameter is actually an approximation of the span from zero volts to V_{FSR} and is equal to $V_{FSR} - 2V_{LSB}$.

$$A_E = \frac{\left(E_{(2^N-2)} - E_0\right) - \left(V_{FS} - 2V_{LSB}\right)}{V_{FS} - 2V_{LSB}} \quad \%/FSR$$

3.8 Integral Linearity Error (I_{LE}). Integral linearity error may be tested at any transition point for the ADC. The total number of points may be very large for higher resolution converters so, generally, the procurement document for the part will specify a limited selection of points for which the measurement is to be made. Zero error and gain for the converter are first obtained from measurements at the end points as in section 3.1 and 3.7. The transition point voltage, E_n, is measured for the nth transition point. Then:

$$I_{LE} = \frac{E_n - V_{IN}(ideal)}{S} \qquad \text{LSB}$$

where gain is given by

$$S = \frac{E_{(2^N-2)} - E_0}{2^N - 2} \qquad \text{Volts/LSB}$$

and $$V_{IN}(ideal) = n_S - Z_E \qquad \text{Volts}$$

3.9 Differential Linearity Error (D_{LE}). Differential linearity error requires two transition point measurements at output codes one binary bit apart. D_{LE} can be measured at any successive pair of transition points and, generally, the procurement document will define a set of points at which the measurement is to be made. The two transition point voltages E_n and $E_{(n-1)}$ are measured at transition points n and (n-1). Then:

$$D_{LE} = \frac{E_n - E_{(n-1)}}{S} \qquad \text{LSB}$$

where gain, S, is obtained as in section 3.8.

3.10 Transition Uncertainty (N_T). The transition uncertainty is obtained by taking a large number of measurements at a specified transition point. The transition point or points at which the measurement is to be made and the minimum number of conversion point measurements to be made will be specified in the procurement document. The transition uncertainity is the span of voltage values from the voltage for which 16% of the conversions occur at a lower voltage and that voltage for which 84% occur at a lower voltage. If the transition point specified for the measurement is n_B and $E_{n(16\%)}$ and $E_{n(84\%)}$ are the transition voltages found from the specified number of transition point measurements, then:

$$N_T = \frac{E_{n(84\%)} - E_{n(16\%)}}{V_{LSB}} \qquad \text{LSB}$$

3.11 Power Supply Sensitivity Ratio (PSSR). The power supply sensitivity is obtained by determining the change in input voltage for a specified transition point when one power supply is varied while the others are held constant. The transition point for the measurement, n_B, and the power supply levels V_{PS}, will be specified in the procurement document. Generally, PSSR is measured at the transition point from all zeros and at the transition point to all ones. If the change in transition point voltages, ΔE_n, measured with power supply levels varied by ΔV_{PS}, then

$$PSSR = = \frac{\Delta E_n}{(\Delta V_{PS}/V_{PS})*100} \qquad \text{LSB/\%PS}$$

3.12 Power Supply Current. Power supply current shall be measured for all device power supplies, including the logic voltage supply. Method 3005.1 of MIL-STD-883C will be used for these measurements. Supply current will be measured for specified output code(s) listed in the procurement document.

3.13 Input Leakage Current (I_{IH}, I_{IL}). Input leakage currents on all logic inputs of the ADC shall be measured using methods 3009.1 (I_{IL}) and 3010.1 (I_{IH}) of MIL-STD-883C.

3.14 Output Voltage Levels (V_{OL}, V_{OH}). Output high (V_{OH}) and low (V_{OL}) voltage levels on the digital outputs shall be measured using methods 3006.1 and 3007.1 of MIL-STD-883C respectively.

3.15 Output High Impedance Current (I_{OZL}, I_{OZH}). Output currents for all digital outputs capable of being placed in high impedance shall be measured using method 3020 for low level current (I_{OZL}), and 3021 for high level current (I_{OZH}). The procurement document will specify the output code that the digital outputs should be set to before being switched to high impedance.

3.16 Output Short Circuit Current (I_{OS}). Output short circuit current will be measured using method 3011.1 of MIL-STD-883C. Output code and duration of the test will be specified in the procurement document.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document for specified values of accuracy and resolution of digitally programmable power supplies and accuracy of the external reference voltage source.

a. V_{FSE} maximum at specified temperature(s).
b. The number of transition points measured for CWE test.
c. Output codes tested for I_{LE}.
d. Output codes tested for D_{LE}.
e. Transition points measured for PSRR.
f. Change in power supply voltage for PSRR test.
g. Output codes used for power supply current measurements, I_{OS}, I_{OZL}, and I_{OZH} tests.
h. Forcing voltages for I_{IH} and I_{IL}.
i. Test limits for all parameters.
j. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25_oC ambient.

Symbol	Transition Code	Analog Input Voltage	Equation	Units
Z_E	0_B	E_0	$V_{LSB} = \frac{V_{FS}}{2^N}$ $Z_E = \frac{E_0}{V_{LSB}}$	LSB
BZ_E	$(2^{N-1}-1)_B$	$E_{(2^{N-1}-1)}$	$BZ_E = \frac{E_{(2^{N-1}-1)}}{V_{LSB}}$	LSB
$-V_{FSE}$	0_B	E_0	$\lvert V_{IN(ideal)}\rvert = \lvert V_{FS}\rvert - V_{LSB}$ $-V_{FSE} = \frac{E_0 - V_{IN(ideal)}}{V_{LSB}}$	LSB
$+V_{FSE}$	$(2^N-2)_B$	$E_{(2^N-2)}$	$+V_{FSE} = \frac{E_{(2^N-2)} - V_{IN(ideal)}}{V_{LSB}}$	LSB
V_{IO}	0_B $1_B, 2_B$	E_0 E_1, E_2	$V_{IO} = E_0 - CWE - V_{LSB}$ $CWE = E_1 - E_2 - V_{LSB}$	Volts
A_E BA_E	$(2^N-2)_B$	$E_{(2^N-2)}$ E_0	$A_E = \frac{(E_{(2^N-2)}-E_0)-(V_{FS}-2V_{LSB})}{V_{FS}-2V_{LSB}} * 100$	$\frac{\%}{FSR}$
I_{LE}	n_B	E_n	$S = \frac{E(2^N-2) - E(0)}{2^N - 2}$ Volts/LSB $V_{IN(ideal)} = nS - \overline{E}$ $I_{LE} = \frac{E_n - V_{IN(ideal)}}{S}$	LSB

Table 1. Equations For A/D Converter Parameters

Symbol	Transition Code	Analog Input Voltage	Equation	Units
D_{LE}	n_B $(n-1)_B$	E_n E_{n-1}	$D_{LE} = \frac{E_n - E_{n-1}}{S}$	LSB
N_T	n_B	$E_{n(84\%)}$ $E_{n(16\%)}$	$N_T = \frac{E_{n(84\%)} - E_{n(16\%)}}{V_{LSB}}$	LSB
PSSR	0_B $(2^N-2)_B$	E_0 $E_{(2^N-2)}$	$PSSR = \frac{\Delta E(n)}{(\Delta V_{PS}/V_{PS})*100}$ V_{PS} = Power Supply Voltage n = 0 or 2^N-2	Volts %FSR

Table 1. Equations For A/D Converter Parameters (Cont.)

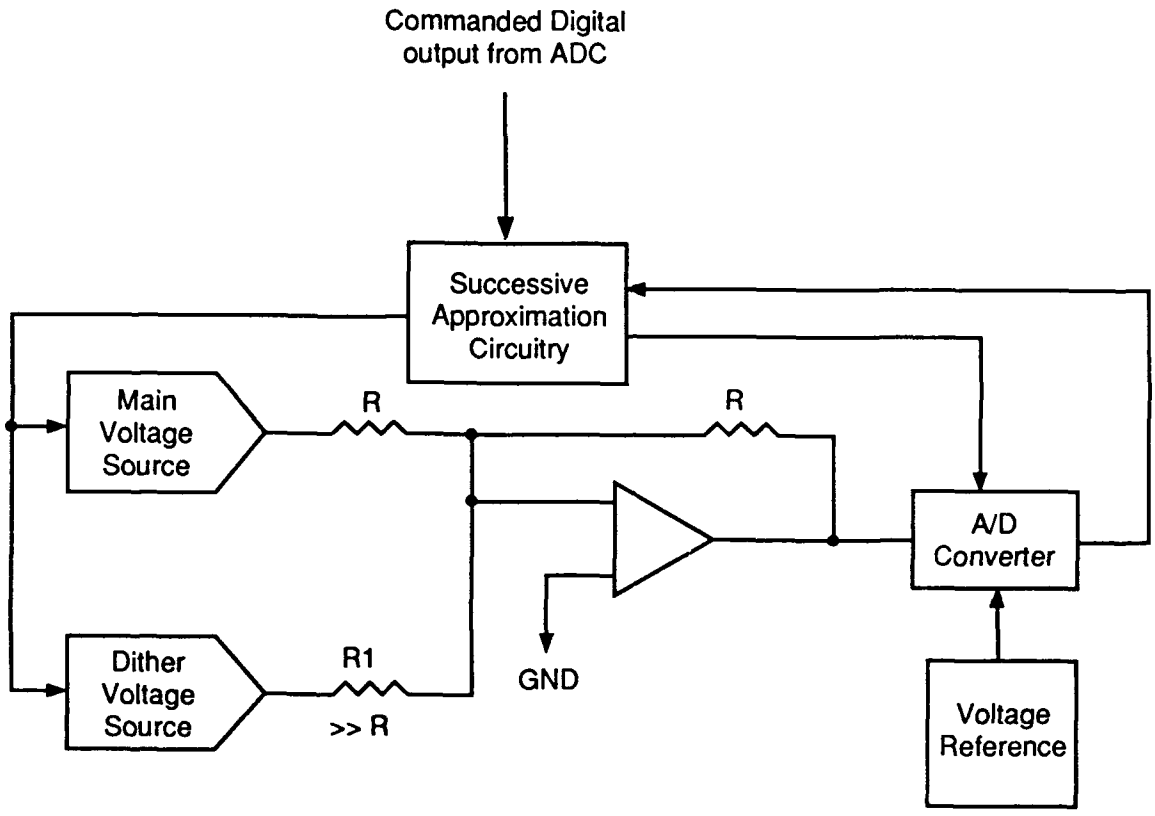


Figure 1. ADC Test Circuit

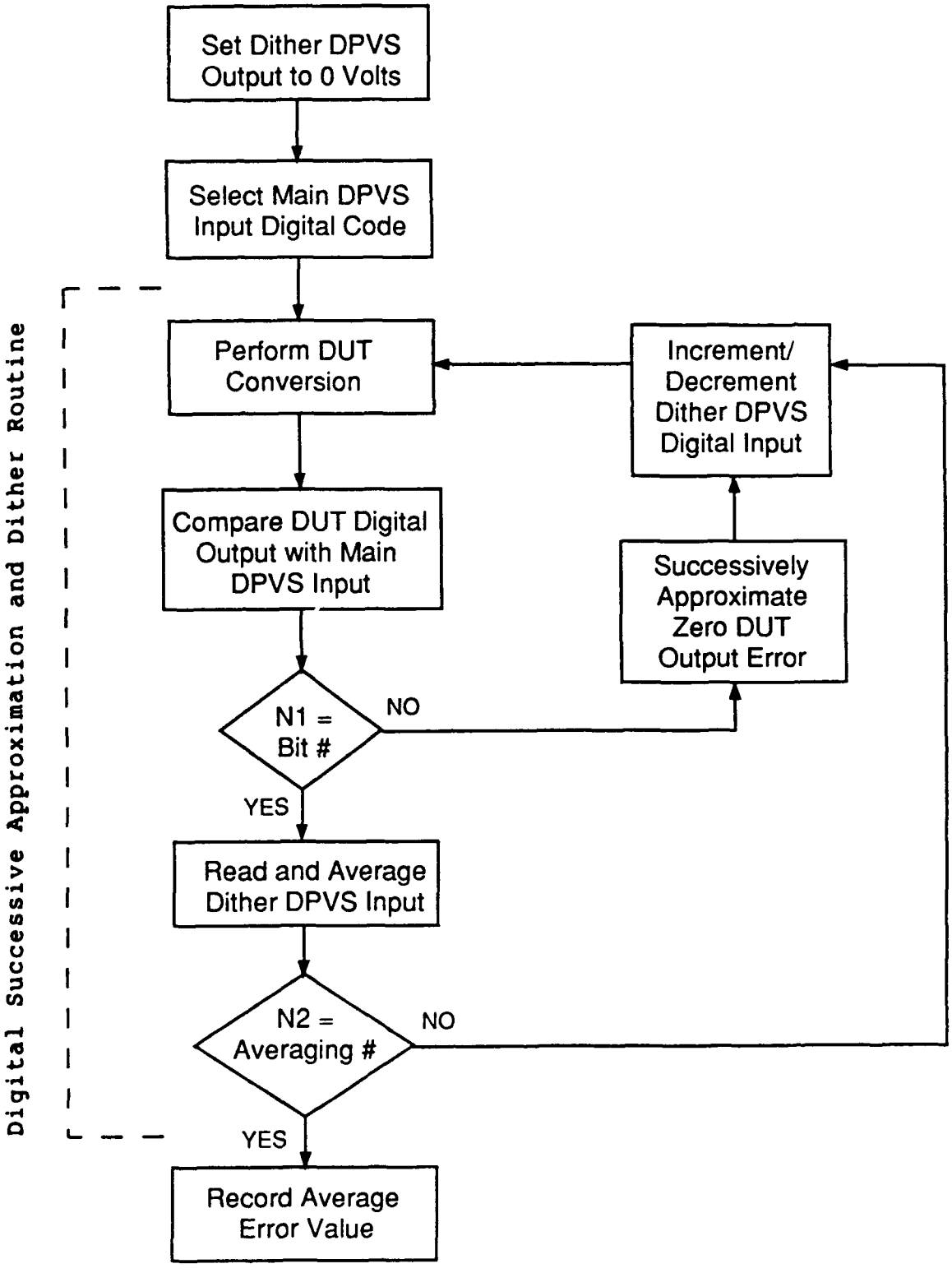


Figure 2. Transition Point Search Routine

VOLTAGE-TO-FREQUENCY CONVERTER TEST METHODS

1.0 PURPOSE. This method establishes the means for measuring offset error, gain, gain error, linearity error and input bias current, low level output voltage, power supply sensitivity and power supply current of integrated circuit voltage-to-frequency converters.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Voltage-to-Frequency Converter (VFC). A voltage-to-frequency converter is an integrated circuit device which produces an output train of pulses having a frequency linearly proportional to the input voltage. The ideal transfer function for a VFC is

$$F_{OUT} = A_V * V_{IN} \qquad \text{kHz}$$

where A_V is the gain of the VFC in kHz/Volt.

1.1.2 Full Scale Input Voltage (V_{FS}). Full scale input voltage is the specified maximum input voltage for the VFC.

1.1.3 Full Scale Range (FSR). The full scale range is the specified range of frequency from zero volts input to V_{FS} input. Because of the non-ideal characteristic of the device, the measured frequency output for V_{FS} input will generally not be identical to specified FSR.

1.1.4 Gain (A_V). The gain of a VFC is defined to be the slope of the line between the frequency measured at full scale voltage input and the frequency measured at 0.1 percent of full scale voltage.

$$A_V = \frac{F_2 - F_1}{0.999 * V_{FS}} \qquad \text{kHz/Volt}$$

where F_2 is the output frequency at V_{FS} voltage input
F_1 is the output at 0.1 percent of V_{FS} voltage input

The gain accuracy is obtained by comparing the measured gain with the ideal gain calculated from specified full scale voltage and full scale frequency range.

1.1.5 Gain Error (A_E). The gain error is the deviation of the full scale output frequency range calculated as the product of the gain and the full scale input voltage from the specified full scale frequency range of the VFC. It is expressed as a percentage of specified full scale range.

$$A_E = (A_V * V_{FS} - FSR) * \frac{100}{FSR} \qquad \%FSR$$

1.1.6 Offset Voltage (V_{OS}). A deviation from the ideal relationship of zero volts input with zero frequency input is called an offset voltage. The transfer characteristic with an offset voltage becomes:

$$F_{OUT} = A_V * (V_{IN} - V_{OS}) \qquad \text{kHz}$$

which gives for the offset voltage

$$V_{OS} = (.001V_{FS}) - \frac{F_1}{A_V} \qquad \text{Volts}$$

where F_1 is the frequency output measured for input voltage equal to 0.1% V_{FS}.

1.1.7 Linearity Error (L_E). Linearity error is defined at any operating frequency as the deviation from a straight line intersecting full scale frequency and 0.1 percent of full scale frequency.

$$L_E = \left[F_n - (V_{INn} - V_{OS})*A_V\right] * \frac{100}{FSR} \qquad \%FSR$$

where F_n is the output frequency at input voltage V_{INn}

1.1.8 Input Bias Current (I_B). The input bias current is the leakage current at the inverting and non-inverting inputs of the operational amplifier or comparator element that forms the input circuit of the VFC.

1.1.9 Low Level Output Voltage (V_{OL}). The low level output voltage is the low state output voltage for an open collector output with specified current sinking.

1.1.10 Power Supply Sensitivity (P_{SS}). Power supply sensitivity is the relative change in output frequency for a specified change in supply voltages.

1.1.11 Settling Time (t_s). The time required after a step change in input voltage for the output frequency of the converter to settle within a specified percentage of the final frequency. This parameter is specified by the manufacturer but is not tested.

2.0 APPARATUS. The apparatus shall consist of a precision programmable voltage source, a precision frequency counter, programmable bias voltage supplies, a precision operational amplifier and resistive and capacitive elements to implement the test circuit of figure 1.

2.1 Input DC Voltage Supply (VS_1). The input voltage supply will be programmable to force full scale positive and negative input voltages (VFS) to an accuracy of 0.01%.

2.2 Output Current Source Load (CS_1). The constant current source load will be programmable to force a specified load current at the output of the device. The current source will have the capability to be switched out of the circuit when not required.

2.3 Bias Power Supplies (+VSS, -VSS). Device power supplies will be programmable to provide +VSS and -VSS voltages at nominal level specified for the device in test and at the levels specified for variation of bias power supply level. The bias power supplies will be accurate to 0.1%.

2.4 Voltmeter (VM1). The voltmeter shall be capable of measuring the output low voltage to an accuracy of 0.01 volt.

2.5 Oscilloscope (OSC). An oscilloscope is required to observe the low voltage output in the switched low state (V_{OL}). Accuracy shall be 10% of V_{OL} measurement requirement.

2.6 Precision Frequency Counter. The precision frequency counter shall be accurate to 0.1%.

2.7 Operational Amplifier. The operational amplifier should be a type having low offset current and offset voltage and a low temperature coefficient. Recommended type is LM108.

2.8 Resistors. Resistors R_A, R_{IN}, R_{B1}, R_{B2}, R_C, and R_t are 1% tolerance, 1/4 watt metal film resistors. R_S and R_L are 5% tolerance, 1/4 watt carbon resistors. Resistors R_{IN}, R_A, R_S, and R_L are programmable resistors, that is they can be switched to different values to accommodate different devices and tests.

2.9 Capacitors. Frequency setting capacitor C_f and timing capacitor C_t are teflon capacitors accurate to 50 ppm. The operational amplifier frequency compensation capacitor, C_s, should be selected to provide an amplifier bandwidth larger than the full scale frequency range of the VFC in test. C_f and C_t are programmable for different values.

3.0 PROCEDURE. Figure 1 shows the generic test configuration for the tests. The VFC in test defined by the outer border is typical of MIL-M-38510/138 Types 01,02 and 03. The VFC defined by the inner block is typical of DESC 5962-87607 and requires the additional circuit components shown within the outer border for the test procedures.

Test procedures are described below and summarized in table 1. In these procedures, input test voltages specified in the procurement document are denoted by the symbol V and subscript. V_{FS} denotes a specified full scale input voltage. Measured output frequencies are denoted by the symbol F with a numerical subscript or subscript n. Wherever forcing voltages or circuit elements are shown as symbols in table 1, the values for the specific device or test are obtained from the procurement document.

3.1 Gain (A_V). In the circuit of figure 1, output frequency is measured for input voltages equal to V_{FS} and 0.1% of V_{FS}, where V_{FS} is specified in the procurement document. The gain is calculated from the formula of section 1.1.4 and is also shown in table 1.

3.2 Gain Error (A_E). The gain error is calculated from the gain A_V obtained as in section 3.1, the specified full scale voltage range V_{FS}, and the specified full scale frequency range using the formula defined in section 1.1.5 (see table 1).

3.3 Offset Voltage (V_{OS}). The offset voltage is obtained from the output frequency measured at 0.1% of V_{FS} input voltage and the gain (A_V) measured in section 3.1, using the formula in table 1.

3.4 Linearity Error (LE). The linearity error at any input voltage V_{INn} is obtained by measuring the frequency output, F_n, for V_{INn}. The error is calculated from the formula of section 1.1.7 (see table 1).

3.5 Input Bias Currents ($+I_B$, $-I_B$). The bias currents are obtained by measuring the shift in offset voltage caused by inserting a resistor at the input tested. To measure $+I_B$, a resistance of value specified in the procurement document is placed at R_S and the output frequency is measured at V_{FS} input at 2% of full scale. The new gain and offset voltage is calculated from these measurements as in sections 3.1 and 3.3 (see table 1). The resulting offset voltage is subtracted from that found in 3.3 and divided by the value of R_S to obtain the bias current. Similarly, $-I_B$ is obtained by increasing the value of resistor R_{IN} by a specified amount. See table 1 for formulas.

3.6 Low Level Output Voltage (V_{OL}). The low level output voltage is measured with the output at a DC low level voltage state, sinking a specified current in the output. Since the output is pulsed, the value of V_{OL} must be measured with an oscilloscope. Value of the timing capacitor C_t and the output frequency must be specified in the procurement document.

3.7 Power Supply Sensitivity (P_{SS}). Power supply sensitivity is measured by setting the output frequency to a specified value by selecting input resistance R_{IN} and timing capacitor C_t and then changing the supply voltages and remeasuring the frequency.

$$PSS = \frac{\Delta F/F}{\Delta V_S/V_S} \qquad \%kHz/\%Volts$$

where $\Delta F/F$ is the percentage change in output frequency
$\Delta V_S/V_S$ is the percentage change in supply voltage

3.8 Power Supply Current (ICC, IEE). Power supply current for +VSS (ICC) and -VSS (IEE) shall be measured as specified in method 3005.1 of MIL-STD-883C.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document.

a. Full scale input voltage (V_{FS}).
b. Full scale frequency range (FSR).
c. Positive and negative bias voltages and logic voltage for each test ($+V_{SS}$ $-V_{SS}$, V_{DD}).
d. Output sink current required for V_{OL} test.
e. Input voltage (V_{IN}) forced for each test.
f. Change in supply voltages required for power supply sensitivity.
g. Resistor values R_A, R_{IN}, R_{B1}, R_{B2}, R_c, R_t, R_S, R_L for each test and device type.
h. Limit values for each parameter tested.
i. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.

PARAMETER	INPUT V_{IN}	CIRCUIT COMPONENT VALUES R_{IN}	R_L	R_S	C_t	R_A	MEASUREMENT METER	VALUE	EQUATION	UNITS
A_V	---	---	---	---	---	---	---	---	$A_V = \left(\frac{F_2 - F_1}{0.999V_{FS}} \right)$	kHz/V
A_E	---	---	---	---	---	---	---	---	$A_E = \left(A_V * V_{FSR} - FSR \right) * \frac{100}{FSR}$	% FSR
V_{OS1}	$0.001V_{FS}$ V_{FS}	R_{IN} R_{IN}	R_L R_L	0 R_S	C_t C_t	R_A R_A	F_{OUT} F_{OUT}	F_1 F_2	$V_{OS1} = 0.001V_{FS} - \left(\frac{F_1}{A_V} \right)$ same for F_2	mV
L_E	V_{INn}	R_{IN}	R_L	R_S	C_t	R_A	F_{OUT}	F_n	$L_E = F_n (V_{INn} - V_{OS}) * \left(\frac{F_2}{V_{FS} - V_{OS}} \right) * \frac{100}{FSR}$	% FSR
$+I_B$	$0.02V_{FS}$ V_{FS}	R_{IN} R_{IN}	R_L R_L	R_S R_S	C_t C_t	R_A R_A	F_{OUT} F_{OUT}	F_3 F_4	$V_{OS2} = 0.02V_{FS} - F_3 * \left(\frac{0.98V_{FS}}{F_4 - F_3} \right)$ $+I_B = \left(\frac{V_{OS2} - V_{OS1}}{R_S} \right)$	NA
$-I_B$	$0.01V_{FS}$ V_{FS}	R_{IN} R_{IN}	R_L R_L	0 0	C_t C_t	R_A R_A	F_{OUT} F_{OUT}	F_5 F_6	$V_{OS3} = 0.01V_{FS} - F_5 * \left(\frac{0.99V_{FS}}{F_6 - F_5} \right)$ $-I_B = \left(\frac{V_{OS3} - V_{OS1}}{R_{IN}} \right)$	nA

TABLE 1 - VOLTAGE-TO-FREQUENCY CONVERTER TESTS

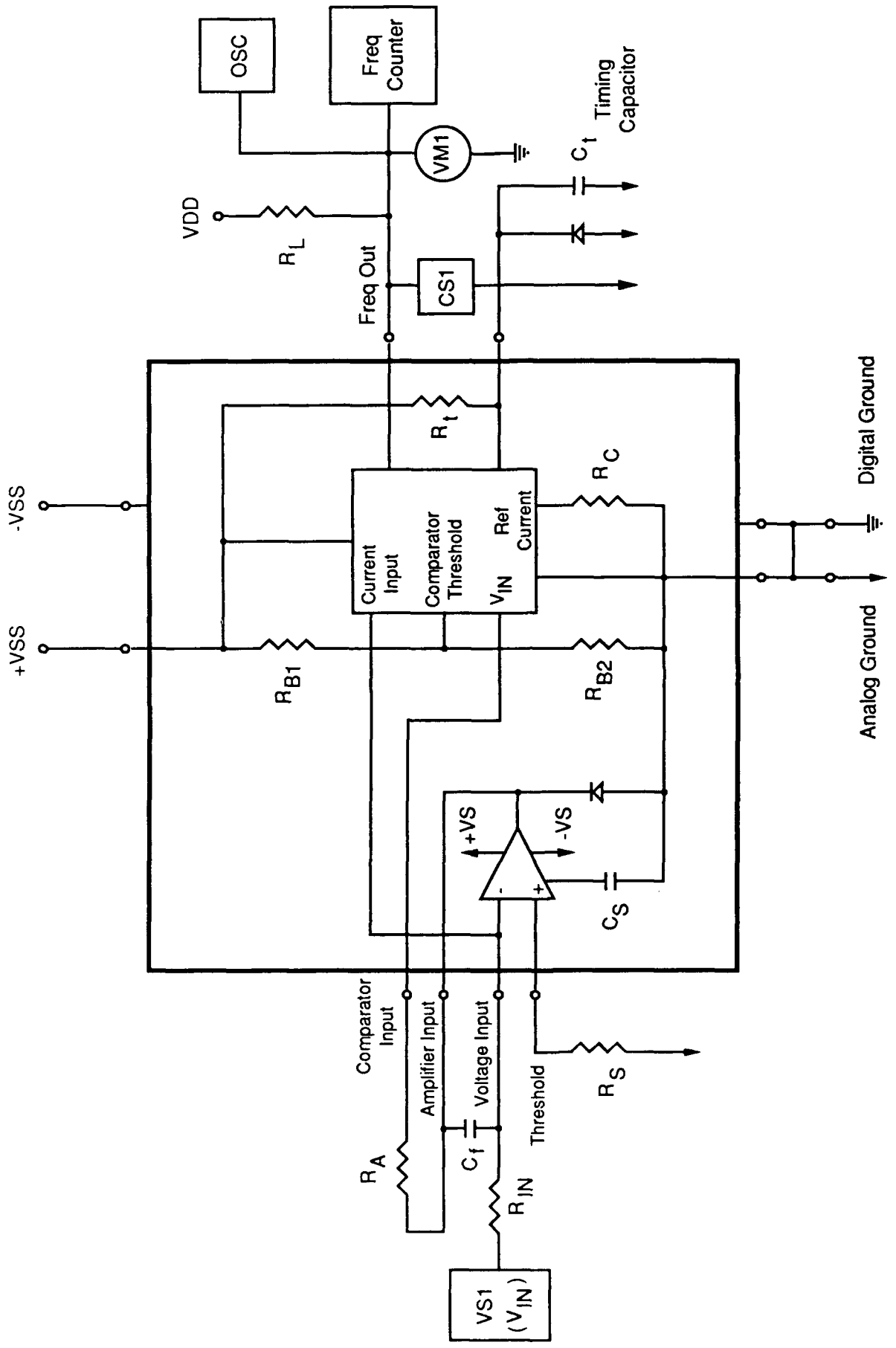


Figure 1. Voltage-to-Frequency Converter Test Circuit

METHOD 4009

FLASH CONVERTER PARAMETERS

1.0 PURPOSE. This method establishes the means for measuring dynamic differential nonlinearity, dynamic integral nonlinearity, signal-to-noise ratio and harmonic distortion of flash A/D converters using a non-coherent digital sampling method.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Flash Converter. A high speed analog-to-digital converter (ADC) made with parallel comparators in which the output code is determined by the number of comparators switched for a given signal level.

1.1.2 Reference Voltage (V_{REF}). An externally or internally supplied voltage which establishes the full scale voltage range of the ADC.

1.1.3 Full Scale Voltages (V_{FS}). The maximum positive and negative voltage inputs that can be resolved by the ADC. These voltages will be some multiple of the internal or external reference voltage supplied to the ADC.

1.1.4 Least Significant Bit (LSB). The lowest order binary bit in the output code of the ADC.

1.1.5 Least Significant Bit Voltage (V_{LSB}). The value in volts of the least significant bit resolved by the ADC. The ideal value of a V_{LSB} is found by dividing the full scale voltage by the magnitude of the binary resolution of the ADC. The ideal value is:

$$V_{LSB} = \frac{VFS}{2^N} \qquad \text{(volts)}$$

where N = number of output bits of the converter

1.1.6 Dynamic Differential Nonlinearity. The deviation in code width from the ideal value of 1 LSB for adjacent codes when measured at data rates representative of normal device operation.

1.1.7 Dynamic Integral Nonlinearity. The deviation of the transfer function measured at representative data rates from an ideal straight line defined by some specified method such as linear regression, or end point to end point.

1.1.8 Signal-to-Noise Ratio. The ratio of the signal output magnitude to the noise plus distortion magnitude expressed as RMS values for a given sample rate and input frequency.

1.1.9 Total Harmonic Distortion (THD). Total harmonic distortion is the difference between an ideal sinewave and its reconstructed version using an A/D converter and a D/A converter or signal processing software by performing

an FFT on the captured digital sampling record. Harmonic distortion can be computed from the ratio of the sum of the squares of the RMS voltage of the harmnics to the RMS voltage of the fundamental. Any number of harmonics can be included in the computation. For example for six harmonics, the harmonic distortion is

$$THD = 20 \log \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, V_6 are the amplitudes of the individual harmonics.

1.1.10 Linear Regression. A mathematical method used to provide a best fit line drawn through a distribution of experimentally derived points.

1.1.11 Code Density. The relative number of occurances of the distinct digital output codes when the part is driven with a specified input signal and the output sampled at a specified rate.

1.1.12 Weighted Code Centers. A process by which groups of output code from an A/D converter arranged in sequence are weighted by their position in the sequence such that out of place codes will have a strong effect on the value of the weighted code. This process makes the statistical center of the step sensitive to the actual or absolute position of each code occurance. Use of weighted codes enables an integral linearity test to reject parts with missing or very misplaced codes.

1.1.13 Sinusoidal Histogram Testing. This test method provides the basis for differential linearity tests and integral linearity tests for Flash A/D converters. With this test method, the DUT samples a specified sinewave input and data samples are captured at the output at a defined rate. A histogram is then computed of code numbers and their frequency of occurance. A plot of differential linearity error and integral linearity error can then be derived. This method is suitable for high frequency testing since the sinewave input can be easily changed to accomodate any frequency. To obtain the sinewave produced histogram the ADC ouput must be sampled at random. To assure that the sinewave input is not sampled repetitively, the sampling frequency is chosen such that it is not harmonically related to the sinewave frequency. If the conversion rate exceeds the rate at which a computer or capture memory can assemble the histogram, every nth sample may be taken since the samples will be selected at random.

1.1.14 Fast Fourier Transform. An algorithm readily implemented with computer software that can perform the discrete Fourier transform relatively rapidly.

1.1.15 Number of Samples. The number of samples needed for estimating the differential nonlinearity or integral nonlinearity based upon the statistical confidence level required.

1.1.16 Probability of ith code for Sinusoid Input P(i). The probability of occurance of a code count for a sinusoidal input waveform, P(i), is given by the expression:

$$P(i) = \frac{1}{\pi} \sin^{-1}\left[\frac{V(i - 2^{N-1})}{A2^N}\right] - \sin^{-1}\left[\frac{V[(i-1) - 2^{N-1}]}{A2^N}\right]$$

where V = full scale range of the ADC
N = number of bits in the ADC
i = code
A = peak amplitude of the input sinewave

2.0 APPARATUS. The apparatus shall consist of a sinewave generator, dc voltmeter, digital data acquisition system, digital signal processor or computer system, and a computer based display system or plotter to display histograms and frequency spectra plots. Also required are device power supplies, reference voltage supplies and control inputs to implement the functional diagram of figure 1.

2.1 Sinewave Generator. The sinewave generator must cover the frequency range of the device under test. The amplitude of the output waveform must be very precisely controlled, for example a digital signal processor might be used in conjunction with a high-speed precision digital-to-analog converter for waveform synthesis.

2.2 DC Voltmeter. The dc voltmeter is used to measure the voltage of the reference input to the A/D converter. The accuracy of the voltmeter should be ten times better than the required accuracy of the voltage reference source.

2.3 Reference Voltage Source. The reference voltage source will be accurate to within 1/2 LSB of the ADC under test. For example, if a 12-bit ADC is to be tested, and the reference voltage is specified to be 10 volts, then the reference voltage source shall be accurate to 1.22 millivolts.

2.4 Data Acquisition System. A parallel input data acquisition system is required to capture the data from the device output. The acquisition system must have an input word width equal to or greater than the number of bits output by the ADC in test, a data acquisition rate equal to the maximum rate of the ADC, and sufficient data storage to collect the required number of data samples.

2.5 Digital Signal Processor or Computer System. A computing system is required to process the captured data and provide the histograms, fast Fourier transforms, and linearity computations required by the this test method specification.

2.6 Computer Graphics Display System or Printer. A graphics display system or printer must be available to provide graphic displays of frequency spectra, histograms, and linearity plots.

2.7 Software. Appropriate software to process histograms and provide for computations such as fast Fourier transforms will be required. Appropriate

routines must also be available to provide plots of differential linearity and integral linearity as a function of code. This should include the ability to provide plots using weighted code centers.

3.0 PROCEDURE. Figure 2 shows the test flow for testing flash converters. Specific tests are outlined in the following sections.

3.1 Dynamic Differential Linearity Error (DLE). Apply an input waveform whose input range is slightly larger than the full scale range of the converter to ensure that all valid output codes are exercised. Sufficient samples must be taken to avoid missing codes and to generate linearity plots with the specified degree of confidence. It is essential that the sinewave be sampled randomly. This can be accomplished by assuring that the sampling frequency is not harmonically related to the sinewave frequency. The data resulting from random sampling will be a distribution of number of counts per code. Code counts for zero code and maximum code should be eliminated. The histogram of the data will then enable detection of missing codes.

Dynamic differential linearity error for any given code is determined by computing the range of input voltages that produce the particular code and weighting this number by the probability of occurance for a sinusoidal waveform:

$$DLE(i) = \frac{\left[\frac{n(i)}{N_t}\right]}{P(i)} - 1 \text{ in LSB}$$

where $n(i)$ = number of counts of code i
N_t = total number of counts
$P(i)$ = Probability of code i occuring (defined in section 1.1.16)

A plot of DLE as a function of code can be made to determine which codes do not meet specification.

3.2 Dynamic Integral Linearity Error (ILE). Integral linearity error for end point to end point (input voltage vs output code) can be computed from differential linearity error by computing an array of ILE(i) values from DLE(i) values. The equation defining this relationship is:

$$ILE(i) = ILE(i-1) + \frac{DLE(i) + DLE(i-1)}{2} \quad \text{in LSB}$$

Integral linearity can be plotted as a function of code so as to determine whether extreme values exceed specification limits. If alternate methods of integral linearity testing are required, such as linear regression or weighted codes, the details must be defined in the procurement document.

3.3. Signal-to-Noise Ratio (S/N). To measure signal-to-noise ratio, an input signal of specified frequency and magnitude must be provided for the gated input of a specified number of complete waveforms. If the number of samples is N, then the number of FFT frequency bins is (N/2 + 1). If specified, multiply collected data by a frequency weighting window, for example a Von Hann window. The computed spectrum is then examined for its fundamental frequency. This section of the spectrum is then removed by setting the frequency bins associated with the fundamental to zero. The RMS of the rest of the spectrum is designated as noise. Signal-to-noise ratio is then determined by computing the ratio of these two RMS voltages and is expressed in decibels.

$$S/N = 20 \text{ LOG } \left[\frac{\text{RMS Signal}}{\text{RMS Noise}}\right]$$

3.5 Harmonic Distortion. To measure harmonic distortion of a device, a spectral response is prepared as for measuring signal-to-noise ratio. The response of the frequency harmonics is then measured for specified harmonics as specified in the procurement document and using the equation shown in section 1.1.9.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document.

a. Input sinewave frequency.
b. Sampling rate and its timing reationship to the input sinewave frequency
c. Frequency weighting window for signal to noise measuements e.g. Von Hann
d. Harmonics to be included in the harmonic distortion measurement.
e. Bias supplies for the part.
f. All load capacitors and resistors used in the tests.
g. Limit values for each parameter tested.
h. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.
i. Specific detail regarding weighted codes and linear regression requirements.

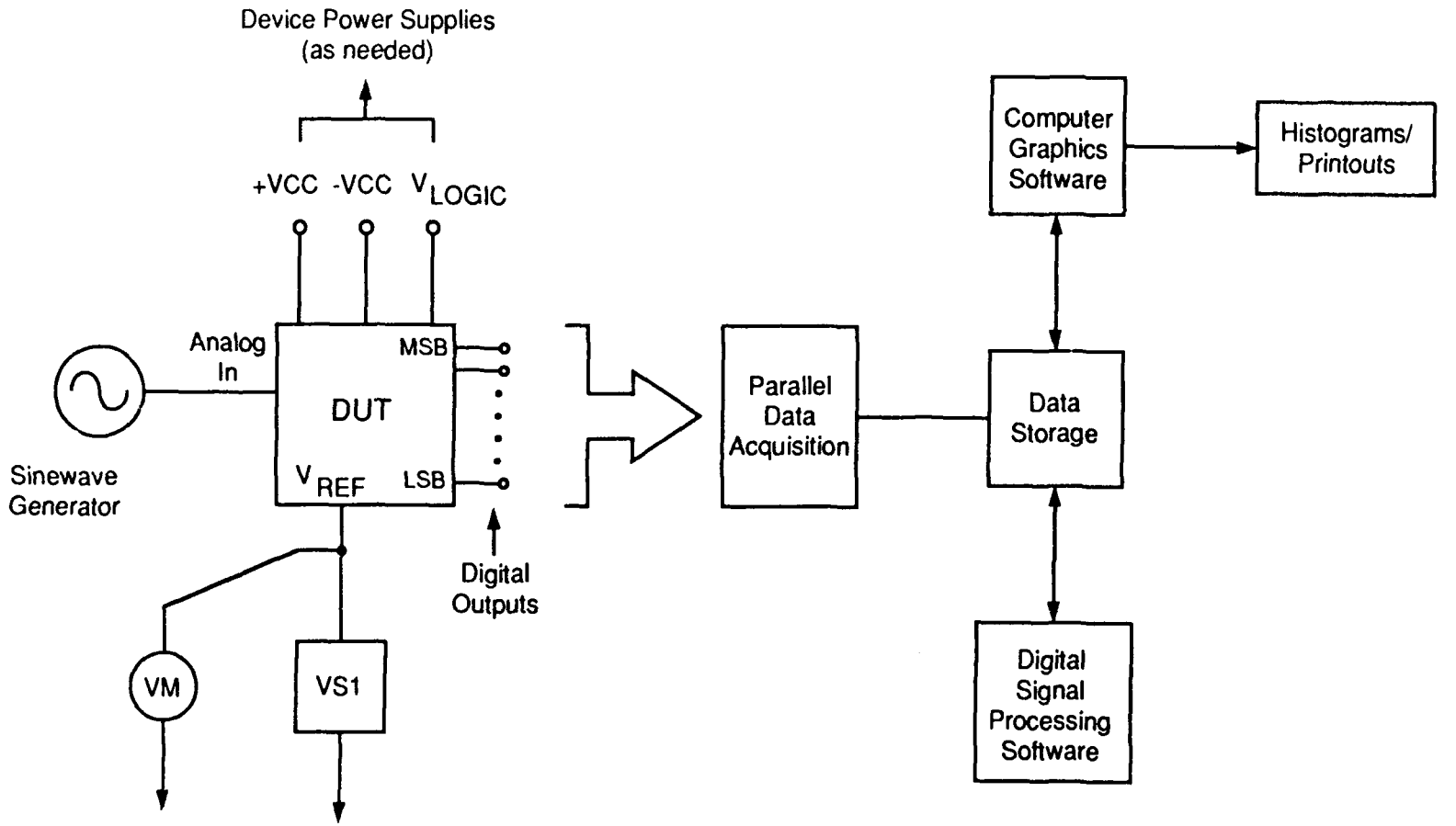


Figure 1. Flash Converter Test Setup

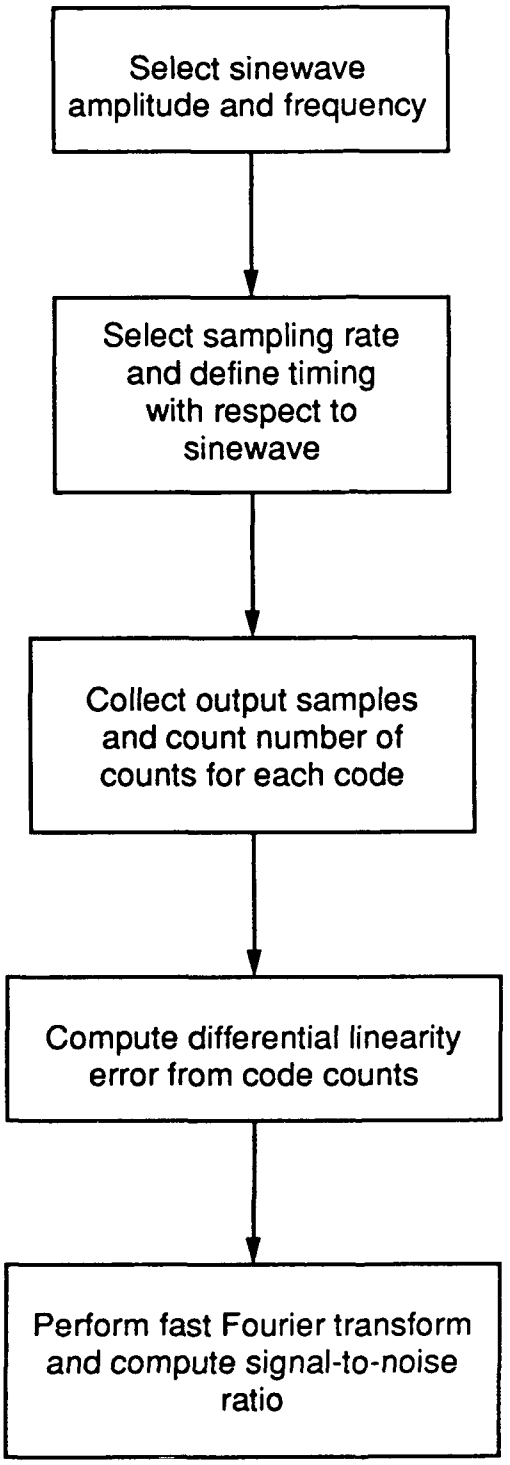


Figure 2. Flash Converter Test Methods Flow Chart

METHOD 4010

ANALOG SWITCH PARAMETERS

1.0 PURPOSE. This method establishes the means for measuring output to input resistance, control input current, input OFF leakage current, output OFF leakage current, output ON current and voltage, channel leakage current, power supply current, charge transfer error, cross talk voltage, OFF isolation voltage, switch on time, switch off time, propagation delay, break-before-make time, and switch capacitance (control, input, and output) of monolithic silicon analog switch integrated circuits comprising one or more switches and including digital control circuitry to gate the switches on and off.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Field Effect Transistor Analog Switch. A field effect transistor switch is a three terminal semiconductor device. An electrically conducting path between the source and drain terminals may be switched on and off by a discrete voltage signal at the input terminal providing that gate-to-source and gate-to-drain voltages retain the proper ploarity and remain within limits. Current carrier flow in the field effect channel is from source to drain and the carriers may be p type or n type depending on the device structure. The sense of the conventional curent (positive to negative) may be into or out of the source terminal depending on the carrier type. This general definition applies to both junction field effect transistors (JFET) and metal-oxide-silicon field effect transistors (MOSFET).

1.1.2. CMOS Analog Switch. A CMOS (complimentary-symmetry metal-oxide-semiconductor) switch is one for which the analog channel is comprised of two MOSFET switches, one p-channel type and one n-channel type, connected in parallel. The advantage of this structure is that the polarity of the gate with respect to the channel terminals is no longer restricted in the switch ON state since one or the other channel will be conducting under all biasing conditions within the range of operation of the device.

1.1.3 Input Terminal. The input terminal is the connection to one end of the conducting channel of the analog switch and is defined as the terminal where the test signals enter the analog switch under test. For a FET switch this is defined to be the Source terminal. For a CMOS switch the input terminal is arbitrarily defined by the functional description of the circuit in the procurement document.

1.1.4 Output Terminal. The output terminal is the connection to the end of the conducting channel other than the input terminal. For a FET switch this is defined to be the drain terminal, and for a CMOS switch it is defined by the functional description of the circuit in the procurement document.

1.1.5 Control Terminal. The control terminal is the connection to the analog switch which controls the gate signal to the FET switch or switches, either directly or indirectly. The control terminal is designated IN_X for JFET switches and CONT X for CMOS switches.

1.1.6 Analog Channel. An electrical path for analog signals. The channel can be switched from a conducting to a non-conducting state by digital signals applied to the control terminal of the analog switch.

1.1.7 ON State. The ON state corresponds to a closed switch with the analog channel conducting.

1.1.8 OFF State. The OFF state corresponds to an open switch with the analog channel not conducting.

1.1.9 Truth Table. A tabulation of the control states required to configure the channels of the analog switch to the ON and OFF states.

1.1.10 Channel Resistance. The resistance between the input and output terminals of the analog switch when the switch is in the ON state.

1.1.11 Control Input Current. The current flowing into or out of the control terminal when either a high state voltage or low state voltage is applied.

1.1.12 OFF Input Current. The leakage current from the input terminal to ground with the analog switch in the OFF state.

1.1.13 OFF Output Current. The leakage current from the output terminal to ground with the analog switch in the OFF state.

1.1.14 ON Output Current. The current flowing into or out of the output terminal with the analog switch in the ON state. This parameter is only applicable to CMOS type switches.

1.1.15 Channel Leakage Current. The combined leakage current from the input and output terminals to ground with the analog switch in the ON state. This parameter is applicable only to FET type switches.

1.1.16 ON Output Voltage. The voltage on the output terminal when a specified current is sourced or sunk and the analog switch is in the ON state. This parameter is specified only for CMOS switches.

1.1.17 Crosstalk Voltage. The degree of cross coupling of a sine wave signal from an ON analog channel to an OFF channel in the same integrated circuit, expressed in dB.

1.1.18 Charge Transfer Error (CTE). This is a measurement of the degree to which the control signal to an analog switch is coupled to the output of the switch. It takes the form of a voltage step (pedestal) appearing on a capacitor at the output of the switch after a transition between ON and OFF states. This voltage is due to charge transfer from the logic control terminal to the switch contact.

1.1.19 OFF Isolation Voltage (V_{ISO}). The ratio of the signal voltage appearing at the output of an OFF channel to the sinusoidal signal voltage applied at the input terminal expressed in dB.

1.1.20 Logic Supply Voltage (V_L). The control logic circuitry supply voltage for the analog switch.

1.1.21 Control Terminal Capacitance (C_{IC}). The capacitance to ground measured at the control terminal.

1.1.22 Switch Input Capacitance (C_{IS}). The capacitance to ground measured at the input terminal of the analog switch.

1.1.23 Switch Output Capacitance (C_{OS}). The capacitance to ground measured at the output terminal of the analog switch.

1.1.24 Switch on Time (t_{on}). The time required for an analog switch to switch from an open state to a closed state after the application of an active signal to the control terminal.

1.1.25 Switch off Time (t_{off}). The time required for an analog switch to switch from a closed state to an open state after the removal of an active signal on the control terminal.

1.1.26 Switch Propagation Delay (t_{PHL}, t_{PLH}). The elapsed time from the application of a signal to the input terminal of an ON analog switch to the time at which the waveform is observed on the output terminal. This parameter is specified for CMOS switches only.

1.1.27 Break Before Make Time (t_D). The difference in time between t_{on} of one analog switch to t_{off} of a second analog switch in the same integrated circuit.

2.0 APPARATUS. The apparatus shall include programmable voltage supplies, programmable current supplies, voltmeters, and current meters to implement the test circuit of figure 1. A pulse generator, sine wave generator and oscilloscope or alternative measuring instrument will be required to implement the circuits of figures 2 through 6. Also, additional programmable voltage supplies to provide the power supply requirements of the analog switch as specified in the procurement document will be needed.

2.1 Input and Output Voltage Supplies (VS_1, VS_2). The input and output voltage supplies will be programmable to force voltage within the range specified for the analog switch input and output terminals at an accuracy of 0.01% and also programmable to an open circuit state, i.e., disconnected from the test device. The power supplies will have separate sense and power inputs/outputs.

2.2 Input and Output Current Supplies (CS_1, CS_2). The input and output current supplies will be programmable to force current within the range specified for the analog switch input and output terminals at an accuracy of 0.1%. The current supplies will also be programmable to an open circuit condition, i.e., zero current.

2.3 Bias Power Supplies. Device power supplies will be programmable to provide V_{DD}, V_{CC} and V_L voltages at nominal level specified for the device in test and at the levels specified for variation of bias power supply level. The bias power supplies will be accurate to 0.1%.

2.4 DC Voltmeters (VM_1, VM_2). The dc voltmeters shall have an input impedance sufficiently high as not to load the circuit under test. Accuracy shall be within 10 percent of the tolerance specified for the circuit tested. For example, if a reading of 0 $\pm$0.1 V is acceptable for the circuit tested, then the voltmeter shall be accurate to within $\pm$0.01 V.

2.5 DC Current Meters (CM_1, CM_2). Current meters used to measure the input and output currents will have an accuracy of 0.1% over the range of currents specified for the analog switch in test.

2.6 Oscilloscope. An oscilloscope may be used to measure on time, off time, break before make time, crosstalk, OFF isolation and charge transfer error. The oscilloscope input impedance will be 1 MΩ or greater and the bandwidth at least ten times the frequency of the square wave specified for the CTE test.

2.7 Sine Wave Generator. This voltage source shall present an effective internal resistance of 50 ohms to the device under test and will be capable of providing a sine wave of specified amplitudes and frequencies for the crosstalk and isolation tests of the analog switch tested.

2.8 Pulse Generator. The pulse generator shall be capable of driving the control terminal of the analog switch with a positive going or negative going logic pulse at a repetition rate of 1 to 10,000 pps.

3.0 PROCEDURE. Figure 1 shows the generic test configuration for the static tests. Figures 2 through 6 show the test circuits used for the dynamic tests. Figure 2 shows the charge transfer error circuit, figure 3 measures crosstalk voltage, figure 4 measures OFF isolation, figure 5 is used for switching tests, and figure 6 illustrates the break-before-make test. Table 1 summarizes the test conditions, measurements and equations for the static tests. For the dynamic tests, this information is included on the drawings or in the descriptive text. In the following procedures, applied test conditions specified in the procurement document are designated with letter subscripts as, for example, V_0 and I_S, while measured values are designated with numerical subscripts as, for example, E_1 and I_1. In all tests, the channel to be tested is set to the specified ON or OFF state by application of the control signals specified in the truth table of the procurement document.

3.1 Channel Resistance (R_{DS}, R_{ON}). Channel resistance is designated Drain-to-Source resistance (R_{DS}) for FET switches and ON resistance (R_{ON}) for CMOS switches. These two measurements are similar. To measure R_{DS}, drain voltage and source current are forced with VS_2 and CS_1 and source voltage is measured as E_1 by VM_1. To measure R_{ON}, input voltage and output current are forced with VS_1 and CS_2 and output voltage is measured as E_2 by VM_2. Where the integrated circuit contains more than one switch, switches not in test are placed in the OFF condition.

$$R_{DS} = \frac{E_1 - V_D}{I_S} \qquad R_{ON} = \frac{V_I - E_2}{I_O}$$

3.2 Control Input Current (I_{IH}, I_{IL}). High level control input current (I_{IH}) is measured using the procedure outlined in method 3010.1 of MIL-STD-883C. Low level current (I_{IL}) is measured using method 3009.1.

3.3 OFF Input Current ($I_{S(OFF)}$, I_{IH}, I_{IL}). OFF input current for CMOS switches is also designated as I_{IH} and I_{IL} and is measured according to methods 3009.1 and 3010.1. For FET switches, this parameter is designated as $I_{S(OFF)}$ and is measured as follows. All switches are set to the OFF state. V_D and V_S are set to specified values by VS_1 and VS_2. $I_{S(OFF)}$ is then measured with current meter CM_1.

3.4 OFF Output Current ($I_{D(OFF)}$). All switches are set to the OFF state. VS_1 and VS_2 are then used to set a specified voltage on the input and output terminals of the analog switch under test. $I_{D(OFF)}$ is then measured using current meter CM_2.

3.5 ON Output Current (I_{OH}, I_{OL}). This measurement is only applicable to CMOS analog switches. ON output current is measured by first placing the switch to be measured in the ON state. VS_2 is then used to place a specified voltage on the output terminal. The resulting current (I_{OH} or I_{OL} depending on the voltage supplied by VS_2) is then measured by CM_2.

3.6 Channel Leakage Current ($I_{D(ON)}$+$I_{S(ON)}$). This measurement applies only to FET switches. To make this measurement the the static parameter test circuit must be modified by removing CS_1, CM_1, and VS_1 from the circuit and connecting the input source to the output drain. The selected switch is then set to the ON state. $I_{D(ON)}$+$I_{S(ON)}$ is then measured using current meter CM_2 with voltage applied using VS_2.

3.7 ON Output Voltage (V_{OH}, V_{OL}). ON Output voltage is only measured for CMOS switches. The switch under test is set to the ON state and V_{OH} is measured using the procedure listed in method 3006.1 of MIL-STD-883C. V_{OL} is similarly measured using method 3007.1.

3.8 Power Supply Current. Power supply current for all device power supplies are measured using the techniques outlined in method 3005.1 of MIL-STD-883C.

3.9 Charge Transfer Error (CTE). Charge transfer error is measured in the circuit of figure 2. The input terminal of the channel is connected to ground and the output terminal is loaded with a capacitor of specified value. The control terminal of the analog switch channel in test is driven with a square wave of specified magnitude, width, frequency, and rise and fall times. The magnitude of the pedestal appearing at the output terminal of the switch in test is the crosstalk error. The measurement may be made with a high impedance oscilloscope (Section 2.6 above) or by a voltage meter having equivalent sampling speed and accuracy.

3.10 Crosstalk Voltage. This test only applies to multiple channel integrated circuits, for example, dual or double throw switches and analog multiplexers. The test circuit is shown in figure 3. A sine wave signal is

forced through an ON switch and transmitted signal strength is measured at an output of an OFF switch. Amplitude and frequency of the sinusoidal signal and load resistors are as specified for the analog switch in test. The output voltage is measured with an oscilloscope or an alternative measurement instrument. Crosstalk voltage is calculated in decibels (db) as:

$$\text{CROSSTALK} = 20*\log \frac{V_{IN}}{V_{OUT}}$$

3.11 OFF Isolation (V_{ISO}). This test measures the leakage of a sine wave signal through an OFF analog switch channel. The test circuit is shown in figure 4. Control inputs are set to open the analog switch channel and a sinusoidal signal of specified amplitude and frequency is applied at the input terminal. The output amplitude is measured with an oscilloscope or alternative measurement instrument. OFF isolation is calculated as:

$$V_{ISO} = 20*\log\left(\frac{V_{IN}}{V_{OUT}}\right)$$

3.12 Switch On Time (t_{on}). This test measures the time required for an analog switch to switch on after the application of an active signal at the control terminal. The test circuit with switching waveforms is shown in figure 5. Switching time is measured from the mid point of the input pulse transition to the 90% point of the output waveform.

3.13 Switch Off Time (t_{off}). This test measures the time required for an analog switch to switch OFF after the removal of a valid signal on control terminal. The test circuit with switching waveforms is shown in figure 5.

3.14 Switch Propagation Delay (t_{PHL}, t_{PLH}). Switch propagation delay is measured with the switch in the ON state. A waveform is applied on the input terminal of the analog switch and the output response monitored on the output terminal. Method 3003.1 of MIL-STD-883C is used to make the measurement.

3.15 Break-Before-Make Time (t_D). For switches consisting of a normally ON channel and a normally OFF channel controlled by the same input, it is usually desired that the ON channel will open before the OFF channel closes. The test circuit and waveforms for the break-before-make time are shown in figure 6.

3.16 Control Terminal Capacitance (C_{IC}). Connect capacitance bridge between the control terminal and reference ground and measure capacitance.

3.17 Switch Input Capacitance (C_{IS}). With the analog switch in the open state, connect capacitance bridge between the switch input terminal and reference ground and measure capacitance.

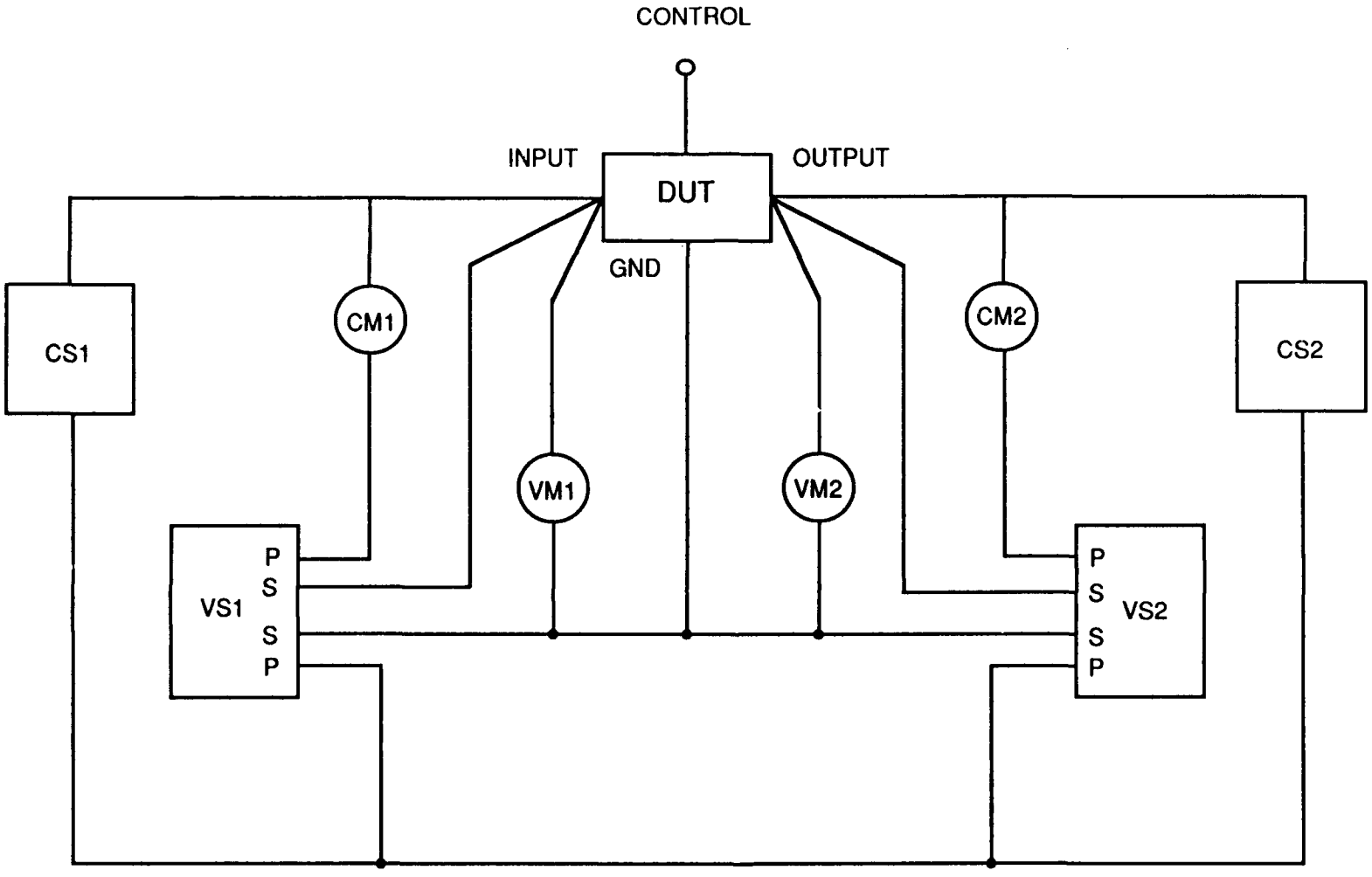
3.18 Switch Output Capacitance (C_{OS}). With the analog switch in the open state, connect capacitance bridge between the switch output terminal and reference ground and measure capacitance.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document.

a. Digital logic truth table.
b. Designation of Input and Output terminals for CMOS switches.
c. Maximum and minimum logic voltage levels over the temperature range tested.
d. Power supply voltage levels for each test.
e. V_{IN}, V_{OUT}, I_{IN}, I_{OUT} forced for each test.
f. Waveform characteristics for CTE input pulse.
g. Waveform characteristics for sinusoidal input for Crosstalk test.
h. Waveform characteristics of sinusoidal input used in V_{ISO}.
i. V_I for break before make test.
j. Test frequency for capacitance measurements.
k. All load capacitors and resistors used in the tests.
l. Limit values for each parameter tested.
m. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.

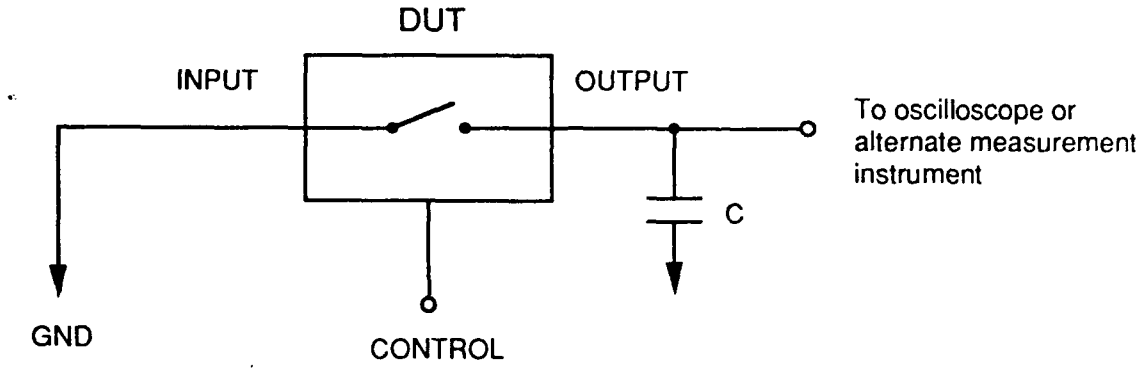
PARAMETER	CHANNEL STATE	FORCED INPUTS VOLTAGE VS_1	FORCED INPUTS CURRENT CS_1	FORCED OUTPUTS VOLTAGE VS_2	FORCED OUTPUTS CURRENT CS_2	MEASUREMENT METER	MEASUREMENT VALUE	EQUATION	UNITS	NOTES
R_{DS}	ON	OPEN	I_S	V_D	OPEN	VM_1	E_1	$R_{DS} = \frac{E_1 - V_D}{I_S}$	OHMS	JFET ONLY
R_{ON}	ON	V_I	OPEN	OPEN	I_O	VM_2	E_2	$R_{ON} = \frac{V_I - E_2}{I_O}$	OHMS	CMOS ONLY
$I_{S(OFF)}$	OFF	V_S	OPEN	V_D	OPEN	CM_1	I_1	$I_{S(OFF)} = I_1$	AMPS	JFET ONLY
$ID_{(OFF)}$	OFF	V_S	OPEN	V_D	OPEN	CM_2	I_2	$I_{D(OFF)} = I_2$	AMPS	
I_{OH}	ON	V_I	OPEN	V_O	OPEN	CM_2	I_3	$I_{OH} = I_3$	AMPS	CMOS ONLY
I_{OL}	ON	0.0V	OPEN	V_O	OPEN	CM_2	I_4	$I_{OL} = I_4$	AMPS	CMOS ONLY
$I_{D(ON)} + I_{S(ON)}$	ON	REMOVED	REMOVED	V_D	OPEN	CM_2	I_5	$I_{D(ON)} + I_{S(ON)} = I_5$	AMPS	JFET ONLY

TABLE 1. ANALOG SWITCH EQUATIONS

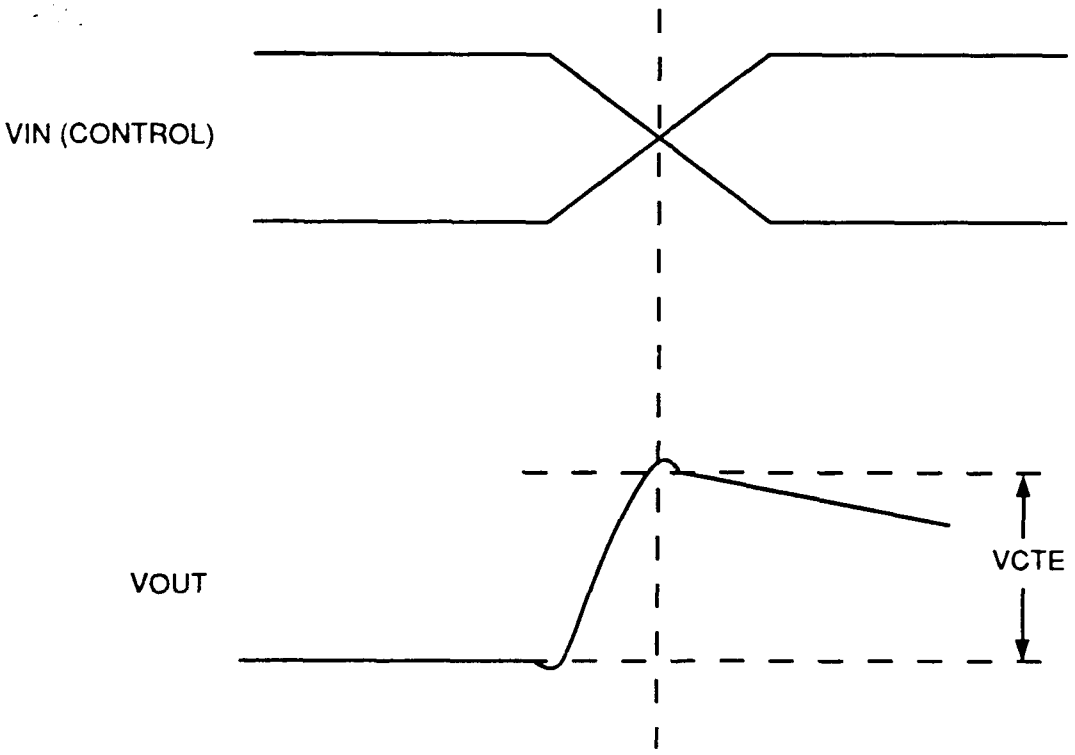


Notes: 1. VSS, VDD, VL (not shown), are referenced to GND
2. Only one of CS1 and CS2 may be required for some circuits

Figure 1. Analog Switch Static Parameter Test Circuit

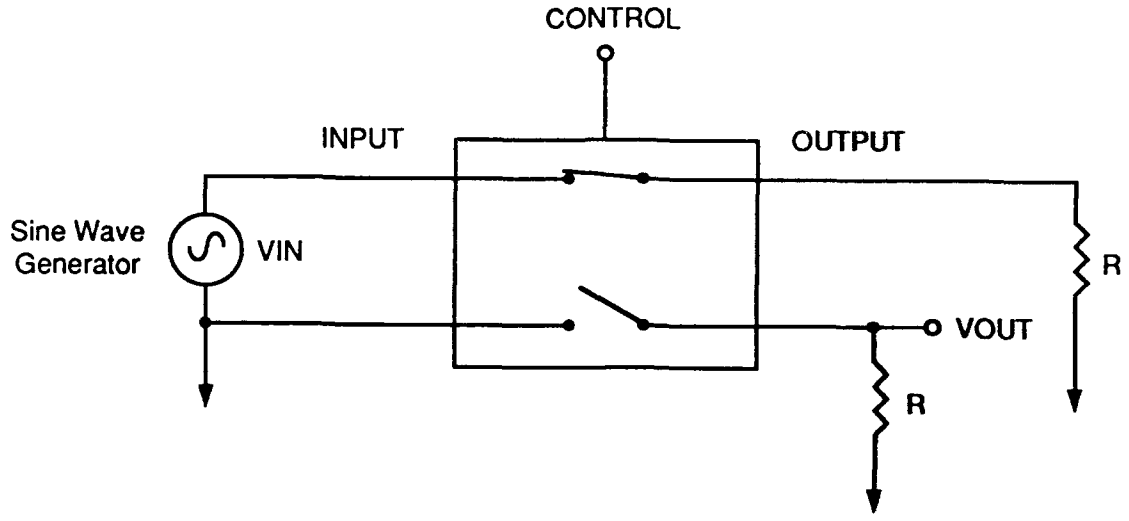


Test Circuit



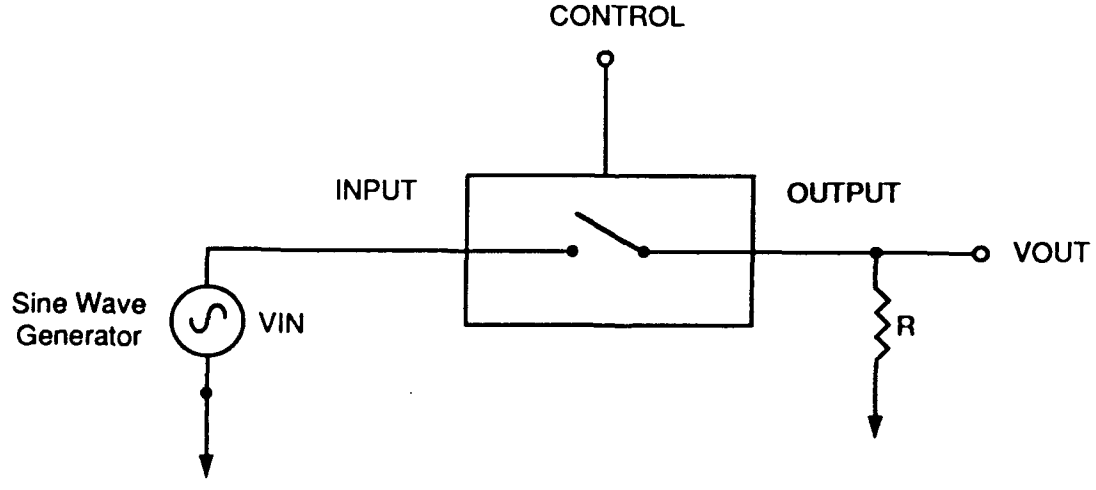
Waveforms

Figure 2. Charge Transfer Test



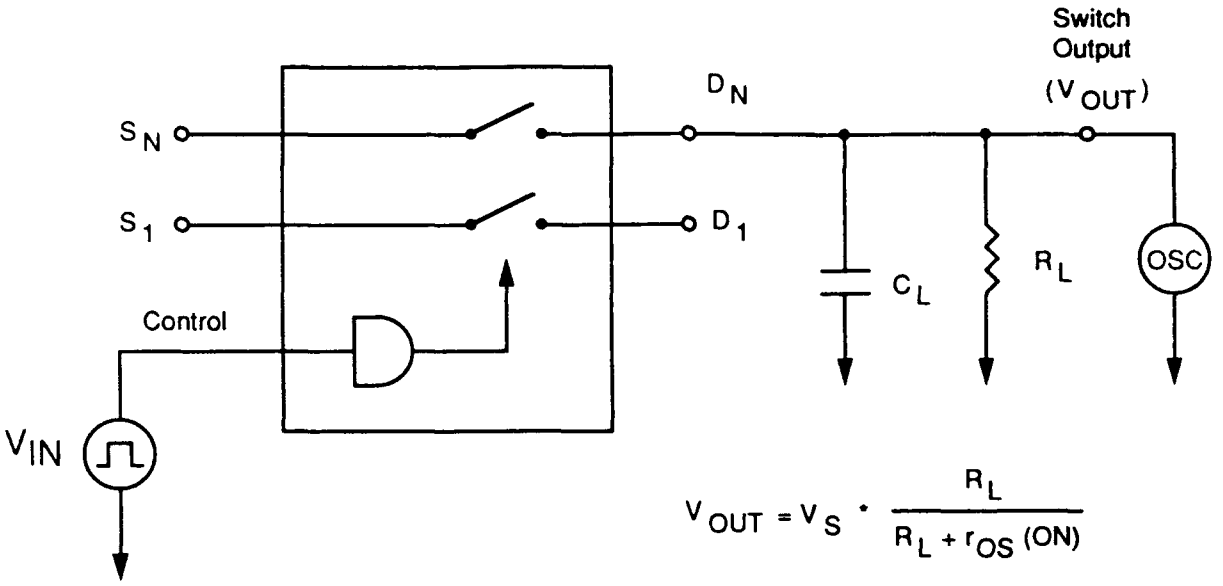
$$\text{Crosstalk} = 20 * \text{Log} \frac{\text{VIN}}{\text{VOUT}}$$

Figure 3. Crosstalk Test Circuit



$$\text{OFF Isolation} = 20 * \text{Log} \frac{\text{VIN}}{\text{VOUT}}$$

Figure 4. OFF Isolation Test Circuit



Notes: 1. Repeat test for other control inputs and S_2 to S_N and D_2 to D_N

2. Invert control input waveform for switches that have the opposite logic sense control

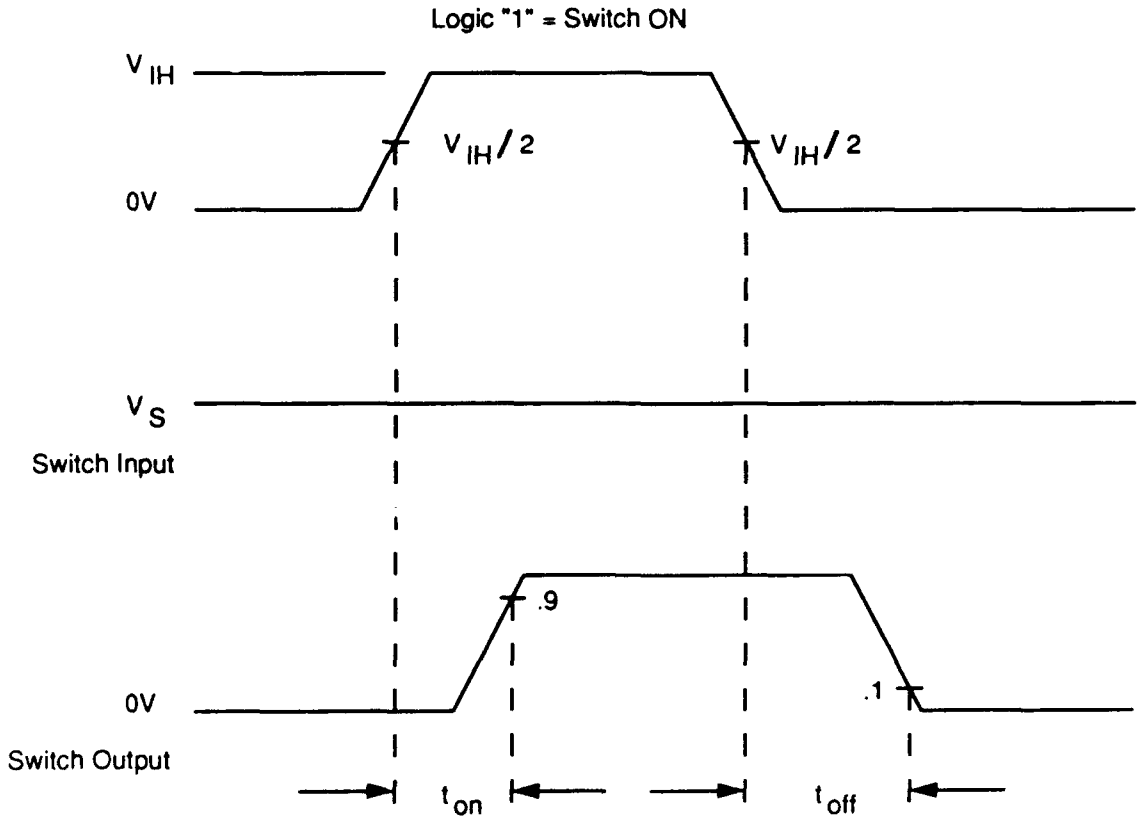


Figure 5. Switching Time Waveforms for t_{on} and t_{off}

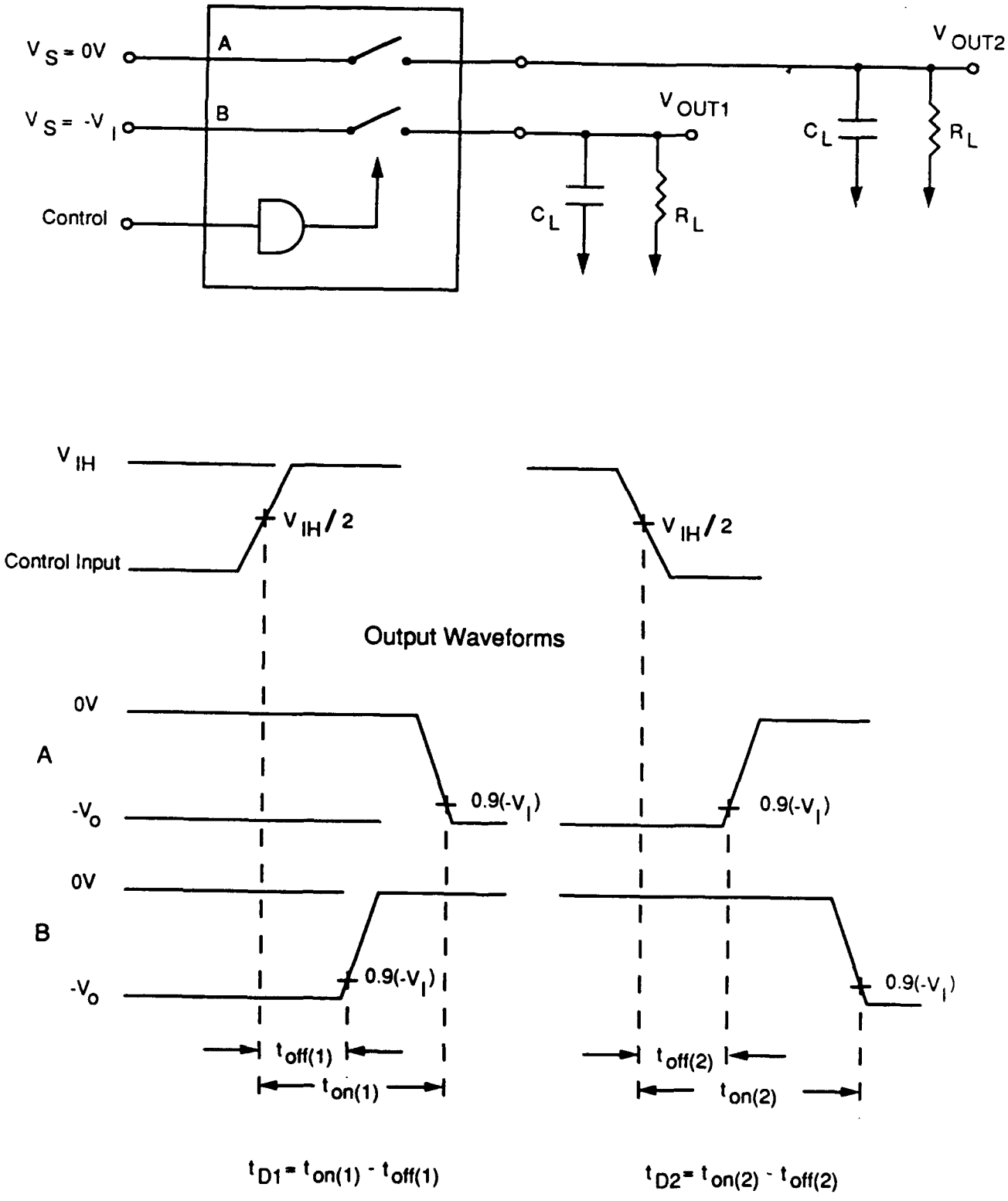


Figure 6. Break-Before-Make Test

METHOD 4011

ANALOG MULTIPLIER

1.0 PURPOSE. This method establishes the means for measuring accuracy, output offset voltage, feedthrough, small signal amplitude error, nonlinearity, input offset voltage, input bias current, input offset current, power supply rejection ratio, common mode rejection ratio, output voltage swing, output short circuit currrent, power supply current, settling time and slew rate of analog multiplier integrated circuits.

1.1 Definitions. The following definitions shall apply for the purpose of this test method.

1.1.1 Analog Multiplier. A linear analog integrated circuit that will accept two or more analog input voltages and output a linearly scaled voltage representing the product, quotient, square, or square root of the input voltages depending on device properties and connections.

1.1.2 Input Voltage. A single ended or differential voltage signal, either fixed or variable, applied at the input terminals of the analog multiplier.

1.1.3 Full Scale Voltage (V_{FS}). The full scale positive or negative input voltage over which the analog multiplier is specified to operate.

1.1.4 Single Ended Input. Single ended input refers to analog multipliers for which the input channels have one input always connected to a common signal ground, usually the power supply common return.

1.1.5 Differential Input. Differential input refers to analog multipliers for which the input channels have two independent terminals, each of which may be biased positive or negative with respect to the signal ground reference level.

1.1.6 Transfer Function. The algebraic expression defining the relationship between the input voltages and the output voltage. The ideal transfer function of an analog multiplier having two inputs, X and Y, is given by the equation:

$$E_o xy = \frac{(Vx)(Vy)}{B} \quad \text{volts}$$

where E_o is the output voltage of the multiplier, Vx, Vy are applied voltages at the inputs, and B is the scale factor of the multiplier.

1.1.7 Four Quadrant Multiplier. An analog multiplier which accepts both positive and negative voltages at each input and produces a scaled algebraic product at the output is said to be a four quadrant multiplier.

1.1.8 Multiplier Accuracy (MA). The difference between the measured output voltage and the ideal output voltage computed from the transfer function, and defined as a percent of full scale output voltage. The multiplier accuracy is the sum of offset voltage, feedthrough and nonlinearity.

1.1.9 Output Offset Voltage (VOIO). The voltage measured at the output of the multiplier with all signal inputs equal to zero.

1.1.10 Feedthrough (FT). Feedthrough error results when one input voltage is zero and a non-zero voltage at the other input causes an output voltage that is in addition to any offset voltage or nonlinearity error. FT is calculated as the measured output voltage, less the offset voltage and nonlinearity error.

1.1.11 Nonlinearity (NL). Nonlinearity occurs when the gain of the multiplying amplifier is different in different quadrants. It is calculated as one half the difference between the the measured plus and minus full scale outputs with feedthrough error and offset voltage eliminated.

1.1.12 Small Signal Amplitude Error (AE). The frequency at which the output from a low level ac signal is reduced from its low frequency level by one percent.

1.1.13 Input Offset Voltage (V_{IO}). The voltage that must be applied between the input terminals of the amplifier to obtain zero output voltage.

1.1.14 Input Bias Currents (I_{IB}). The current into an input terminal when the output is at zero volts.

1.1.15 Input Offset Currents (I_{IO}). The difference between the currents into the two input terminals of a differential input when the output is at zero volts.

1.1.16 Power Supply Rejection Ratio (PSRR). The inverse ratio of the change in output voltage to a change in the power supply voltage. It is specified in decibels.

1.1.17 Common Mode Rejection Ratio (CMRR). The ratio of the common mode voltage range to the change in output voltage over this range. CMRR is specified for a specific common mode voltage range.

1.1.18 Output Voltage Swing (V_{OP}). The peak output voltage that can be obtained without clipping into a specified load resistance.

1.1.19 Settling Time (t_s). The time after the application of a step input voltage change for the output to settle to within a specified error band of the final output voltage.

1.1.20 Slew Rate (SR). The ratio of a change in output voltage to the time required to effect this change under large-signal drive conditions. Slew rate may be specified separately for positive and negative going changes.

1.1.21 Wideband Noise (NI(BB)). The unfiltered rms noise voltage at the output of the amplifier when both inputs are at zero volts.

2.0 APPARATUS. The apparatus shall include programmable voltage supplies, sine wave generators, a dc voltmeter, and an oscilloscope or alternative measuring instruments to implement the circuit of figure 1. Also, additional programmable voltage supplies to provide the power supply requirements of V_{CC} and V_{EE} for the analog multiplier as specified in the procurement document.

2.1 Input DC Voltage Supplies (VS_1, VS_2, VS_3, VS_4). The input voltage supplies will be programmable to force full scale positive and negative voltages (VFS) and zero volts for the analog multiplier with an accuracy of 0.1% and also programmable to an open circuit state, i.e., disconnected from the test device. The power supplies will have separate sense and power inputs/outputs.

2.2 Bias Power Supplies (V_{CC}, V_{EE}). Device power supplies will be programmable to provide V_{CC} and V_{EE} voltages at nominal levels specified for the device in test and at the levels specified for variation of bias power supply level. The bias power supplies will be accurate to 1.0%.

2.3 DC Voltmeter (VM1). The dc voltmeter shall have an input impedance sufficiently high as not to load the circuit under test. Accuracy shall be within 10 percent of the tolerance specified for the circuit tested. For example, if a reading of 0 $\pm$0.1 V is acceptable for the circuit tested, then the voltmeter shall be accurate to within $\pm$0.01 V.

2.4 Function Generators (VS_5, VS_6). These voltage sources shall present an effective internal resistance of 50 ohms to the analog multiplier under test and will be capable of providing a sine wave of specified amplitude and frequency for the small signal amplitude error test and also a square wave of amplitude specified for the settling time and slew rate tests.

2.5 AC Voltmeter or Oscilloscope (VM2). The ac voltmeter or oscilliscope used to measure the amplitude of the sine wave at the output of the analog multiplier should have an input impedance of 1 megohm or greater and bandwidth of at least ten times the frequency for the small signal amplitude error specified for the analog multiplier in test.

2.6 RMS Voltmeter (VM3). The rms voltmeter used to measure wideband noise should have a bandwidith of 10 Hz to 100 kHz or higher and be capable of measuring rms voltage to an accuracy of 0.1 mV.

3.0 PROCEDURE. Figure 1 shows the generic test circuit for testing analog multipliers having two inputs, X and Y. The device depicted is a differential input, four quadrant analog multiplier, but the circuit also applies to single ended and two quadrant devices. All tests are performed in single ended configuration with differential input analog multipliers having one terminal of a differential input at signal ground reference level in each test. The external offset adjustment terminal, VOS, of the analog multiplier is connected to ground during the tests. Load resistor and

capacitor values R_L and C_L will be as specified in the procurement document. Power supplies should be adequately decoupled from the DUT (device under test).

Test procedures are summarized in table 1. In the procedures below and in table 1, input test voltages specified in the procurement document are denoted by the symbol V and subscript. VFS denotes a specified full scale input voltage. Measured output voltages are denoted by the symbol E.

3.1 Multiplier Accuracy (MA). Multiplier accuracy is tested for each quadrant in which the multiplier is specified to operate. Multiplier accuracy for different quadrants is designated with the polarity of the input x and y voltages. For example, MAx-y- denotes multiplier accuracy measured with negative voltage on both inputs. The direction of polarity for the differential inputs of a multiplier will be specified in the procurement document. Voltage inputs for the multiplier accuracy tests are full scale positive and negative input voltages.

Multiplier accuracy is calculated as,

$$MAxy = \left(\frac{(Vx)(Vy)}{B} - E_o \right) * \frac{100}{FSR} \qquad \%/FSR$$

where Vx, Vy are applied voltages at inputs, B is the scale factor of the multiplier, and E_o is the measured output voltage of the multiplier.

3.2 Output Voltage Offset (VOIO). Output offset voltage is measured as the multiplication error with Vx and Vy both set to zero. The measured output voltage, E, is equal to VOIO.

3.3 Feedthrough Error (FT). Feedthrough error is tested for each input to the multiplier as FTx and FTy. FTx is measured with the Y input held at zero voltage. The output voltage is measured with positive and negative full scale voltages at the X input of the analog multiplier and these measurements are averaged. The output offset voltage is subtracted from the result to obtain the feedthrough error.

$$FTx = \frac{(Ex+) + (Ex-)}{2} - VOIO \qquad volts$$

where FTx is the feedthrough error for the X input, Ex+ is the output voltage measured with Vx = +VFS, Ex- is the output voltage measured with Vx = -VFS and VOIO is the measured output offset voltage

Feedthrough error at input Y, FTy, is measured similarly.

3.4 Nonlinearity (NL). Nonlinearity is measured for positive and negative full scale voltages on each input. The effect of feedthrough from the other input is cancelled by making two measurements of output voltage; first with full scale positive applied at the input not tested and then with full scale negative voltage applied. The result of the two measurements is

averaged and the feedthrough term is then subtracted. The resulting nonlinearity error is divided by two to obtain a best line through the error curve. The result is converted to a percent of full scale.

The equation is given below for the measurement of NLx+ which is the nonlinearity for a full scale positive input voltage at the X input.

$$NLx+ = \frac{[(Ex+y+) + (Ex+y-)]/2 - XFP}{2} \quad \text{volts}$$

where NLx+ is the nonlinearity error for positive X input voltage, Ex+y+ is the output voltage measured with Vy = +VFS, Ex+y- is the output voltage measured with Vy = -VFS and XFP is the measured output when X = +10 and Y = 0.

Nonlinearity tests for NLx-, NLy+ and NLy- are made similarly.

3.5 Small Signal Amplitude Error (AE). Small signal amplitude error is measured by applying a sine wave signal of specified amplitude and frequency to the X or Y terminal while a full scale dc voltage is applied to the alternate terminal. Output amplitude, E_o, is measured at the specified frequency, f_o, and the frequency of the signal is then increased until the measured ac output voltage is reduced by one percent from the original reading.

3.6 Input Offset Voltage (V_{IO}). To measure input offset voltage $V_{IO}(x)$, zero voltage is applied across the x input terminals and the multiplication error is measured with plus and minus full scale input applied at the y terminals. $V_{IO}(x)$ is calculated as 1/2 the difference between the two multiplication errors:

$$V_{IO}(x) = \frac{E_1 - E_2}{2} \quad \text{volts}$$

where E_1 is the multiplication error for y input equal to plus full scale voltage and E_2 is the multiplication error for y input equal to minus full scale voltage.

$V_{IO}(y)$ is measured similarly.

3.7 Input Bias Currents (I_{IB}). Bias currents are measured at each input of the analog multiplier with all input voltages set to zero volts. Table 1 indicates the measurement made and formula for each input bias current of a differential input analog multiplier.

3.8 Input Offset Currents (I_{IO}). Input offset currents are measured for differential input analog multipliers as the difference between the current into the positive (non-inverting) input for one channel and the current into the negative (inverting) input.

3.9 Power Supply Rejection Ratio (PSRR). To measure the power supply rejection ratios, specified V_x and V_y are applied at the input terminals of the analog multiplier, output voltage is measured with V_{CC} and V_{EE} at nominal values and with V_{CC} and V_{EE} decreased or increased in magnitude by a similar amount. Power supply levels and formulae for calculating PSRR are shown in Table 1.

3.10 Common Mode Rejection Ratio (CMRR). Common mode rejection is measured for each differential input pair of the analog multiplier in test. CMRR(x) is measured with a full scale positive input applied at the y channel inputs. Measurements of output voltage are made with the x input common mode voltage at zero volts, + full scale volts, and - full scale volts. The output voltages for full scale input voltages are each compared with the output voltage for zero volts input. The largest ΔE is used to calculate CMRR(x) as follows:

$$CMRR(x) = 20*\log\left(\frac{V_{FS}}{\Delta E}\right) \qquad \text{decibels}$$

CMRR(y) is measured similarly.

3.11 Output Voltage Swing (V_{OP}). V_{OP} is measured by applying overvoltages of $\pm(V_{FS} + 1)$ volt at the y channel while the x channel is held at $V_{FS} + 1$ volt. The output voltages in each case must meet the maximum and minimum specified in the procurement document for the analog multiplier.

3.12 Power Supply Current (ICC, IEE). Power supply current for VCC (ICC) and VEE (IEE) shall be measured using the method outlined in method 3005.1 of MIL-STD-883C.

3.13 Output Short Circuit Current (I_{OS}). Output short circuit current is measured using the procedure outlined in method 3011.1 of MIL-STD-883C. Two such measurements must be made. One with the output voltage of the multiplier at a specified positive value ($I_{OS}(+)$), and one with output voltage at a specified negative value ($I_{OS}(-)$). The duration of the transient short circuit on the output will be specified in the procurement document.

3.14 Settling Time (t_s). Settling time is measured by applying a $\pm V_{FS}$ square wave, as specified in the detailed specification, from the function generator VS_5 of figure 1. The output waveforms are observed on the oscilloscope and the settling times for the negative going and positive going transitions are determined as shown in the transient response waveform of figure 2.

3.15 Slew Rate (SR). Slew rates are measured by applying the same square wave as in the settling time measurement. The positive going and negative going slew rates are measured on the oscilloscope as shown in figure 2.

3.16 Wideband Noise (NI(BB)). Wideband noise is measured in the circuit of figure 3 with voltmeter VM_3 specified in section 2.6 above.

4.0 SUMMARY. The following details shall be specified in the applicable procurement document.

a. Full scale positive and negative input voltages (V_{FS+}, V_{FS-}).
b. Load resistance and capacitance (R_L, C_L).
c. V_{CC}, V_{EE} for each test.
d. Vx, Vy forced for each test.
e. Low frequency, f_o, for amplitude error test.
f. ΔVCC and ΔVEE for PSRR tests.
g. Duration of transient short for I_{OS} test.
h. Waveform characteristics for t_s and SR tests.
g. Limit values for each parameter tested.
h. Test temperature(s). Unless otherwise specified, all parameters shall be measured at the minimum and maximum specified operating temperatures and at 25°C ambient.

PARAMETER	FORCED INPUTS						MEASUREMENT		EQUATION	UNITS
	VS_1	VS_2	VS_3	VS_4	VS_5	VS_6	METER	VALUE		
MAx-y-	-VFS	0	-VFS	0	---	---	VM_1	E_1	$MAx\text{-}y\text{-} = \frac{(E_1 - VFS)}{VFS} * 100$	%FS
MAx-y+	-VFS	0	+VFS	0	---	---	VM_1	E_2	$MAx\text{-}y\text{+} = \frac{(E_2 + VFS)}{VFS} * 100$	%FS
MAx+y-	+VFS	0	-VFS	0	---	---	VM_1	E_3	$MAx\text{+}y\text{-} = \frac{(E_3 + VFS)}{VFS} * 100$	%FS
MAx+y+	+VFS	0	+VFS	0	---	---	VM_1	E_4	$MAx\text{+}y\text{+} = \frac{(E_4 - VFS)}{VFS} * 100$	%FS
VOIO	0	0	0	0	---	---	VM_1	E_5	$VOIO = E_5$	mV
FTx	-VFS +VFS	0 0	0 0	0 0	--- ---	--- ---	VM_1 VM_1	E_6 E_7	$FTx\text{-} = \frac{(E_6 + E_7)}{2} - E_5$	mV
FTy	0 0	0 0	-VFS +VFS	0 0	--- ---	--- ---	VM_1 VM_1	E_8 E_9	$FTy\text{-} = \frac{(E_8 + E_9)}{2} - E_5$	mV
+NLx	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	$+NLx = \frac{(E_4+E_2)/2-E_9}{2*VFS} * 100$	%FS
-NLx	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	$-NLx = \frac{(E_3+E_1)/2-E_8}{2*VFS} * 100$	%FS
+NLy	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	$+NLy = \frac{(E_4+E_3)/2-E_7}{2*VFS} * 100$	%FS
-NLy	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	--- ---	$-NLy = \frac{(E_1+E_2)/2-E_6}{2*VFS} * 100$	%FS
AEx	---	0	+VFS	0	2 Vp-p	---	VM_2	f_1	$AEx = f_1 @ (-1\%) E_o$	kHz
AEy	+VFS	0	---	0	---	2 Vp-p	VM_2	f_2	$AEy = f_1 @ (-1\%) E_o$	kHz

Table 1. Analog Multiplier Equations

PARAMETER	FORCED INPUTS						BIAS		MEASUREMENT		EQUATION	UNITS
	VS_1	VS_2	VS_3	VS_4	VS_5	VS_6	V_{CC}	V_{EE}	METER	VALUE		
$V_{IO}(x)$	0	0	-VFS	0	---	---	+15	-15	VM1	E10	$V_{IO}(x) = \frac{(E10 - E11)}{2}$	volts
	0	0	+VFS	0	---	---	+15	-15	VM1	E11		
$V_{IO}(y)$	-VFS	0	0	0	---	---	+15	-15	VM1	E12	$V_{IO}(y) = \frac{(E12 - E13)}{2}$	volts
	+VFS	0	0	0	---	---	+15	-15	VM1	E13		
$+I_{IB}(x)$	---	0	0	0	---	---	+15	-15	IM1	I1	$I_{IB}(x) = I1$	μA
$-I_{IB}(x)$	0	---	0	0	---	---	+15	-15	IM2	I2	$I_{IB}(y) = I2$	μA
$I_{IO}(x)$	0	0	0	0	---	---	+15	-15			$I_{IO}(x) = I2 - I1$	μA
$+I_{IB}(y)$	0	0	---	0	---	---	+15	-15	IM3	I1	$I_{IB}(x) = I3$	μA
$-I_{IB}(y)$	0	0	0	---	---	---	+15	-15	IM4	I2	$I_{IB}(y) = I4$	μA
$I_{IO}(y)$	0	0	0	0	---	---	+15	-15			$I_{IO}(y) = I4 - I3$	μA
CMRR(x)	-VFS	-VFS	+VFS	0	---	---	+15	-15	VM1	E14	CMRR(x) = 20*log[VFS/ΔV(x)]	db
	0	0	0	0	---	---	+15	-15	VM1	E15	where ΔV(x) = greater of	
	+VFS	+VFS	0	0	---	---	+15	-15	VM1	E16	(E14 - E15) or (E15 - E16)	
CMRR(y)	+VFS	0	-VFS	-VFS	---	---	+15	-15	VM1	E17	CMRR(y) = 20*log[VFS/ΔV(y)]	db
	0	0	0	0	---	---	+15	-15	VM1	E18	where ΔV(y) = greater of	
	+VFS	0	+VFS	+VFS	---	---	+15	-15	VM1	E19	(E17 - E18) or (E18 - E19)	
PSRR1	+VFS/2	0	+VFS	0	---	---	+15-ΔV	-15+ΔV	VM1	E20	$PSRR1 = \frac{(E20 - E21)}{\Delta V}$	volts
	+VFS/2	0	+VFS	0	---	---	+15	-15	VM1	E21		
PSRR2	+VFS/2	0	+VFS	0	---	---	+15+ΔV	-15-ΔV	VM1	E22	$PSRR2 = \frac{(E22 - E23)}{\Delta V}$	volts
	+VFS/2	0	+VFS	0	---	---	+15	-15	VM1	E23		
V_{OP1}	+VFS+1V	0	+VFS+1V	0	---	---	+15	-15	VM1	E24	$V_{OP} = E24$	V
V_{OP2}	+VFS+1V	0	-VFS-1V	0	---	---	+15	-15	VM1	E25	$V_{OP} = E25$	V
t_s	---	0	---	0	V_{p-p}^{20} f = 10 kHz	---	+15	-15	OSC	$t_s(+)$ $t_s(-)$	see figure 3 waveform	μs μs
SR(+)	---	0	---	0	V_{p-p}^{20} f = 10 kHz	---	+15	-15	OSC	SR(+)	see figure 3 waveform $SR(+) = \frac{\Delta V_o(+)}{\Delta t(+)}$	μs
SR(-)	---	0	---	0	V_{p-p}^{20} f = 10 kHz	---	+15	-15	OSC	SR(-)	see figure 3 waveform $SR(-) = \frac{\Delta V_o(-)}{\Delta t(-)}$	μs

Table 1 (continued). **Analog Multiplier Equations**

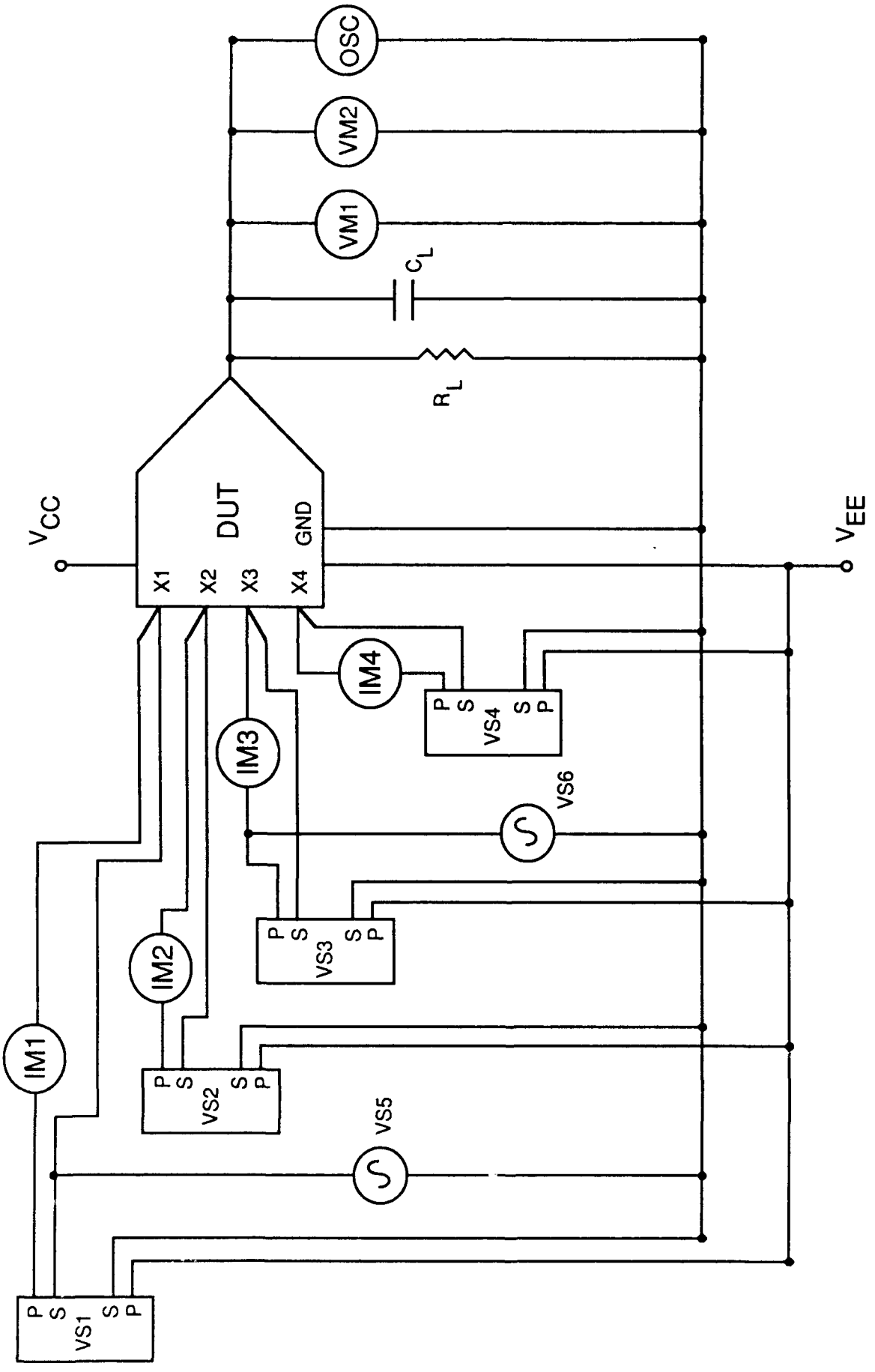
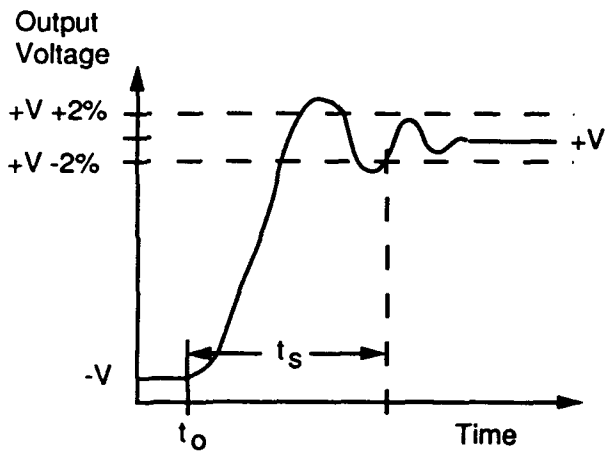
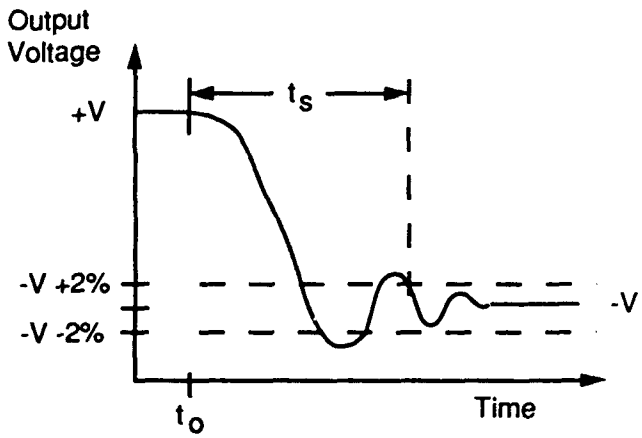


Figure 1. Analog Multiplier Test Circuit



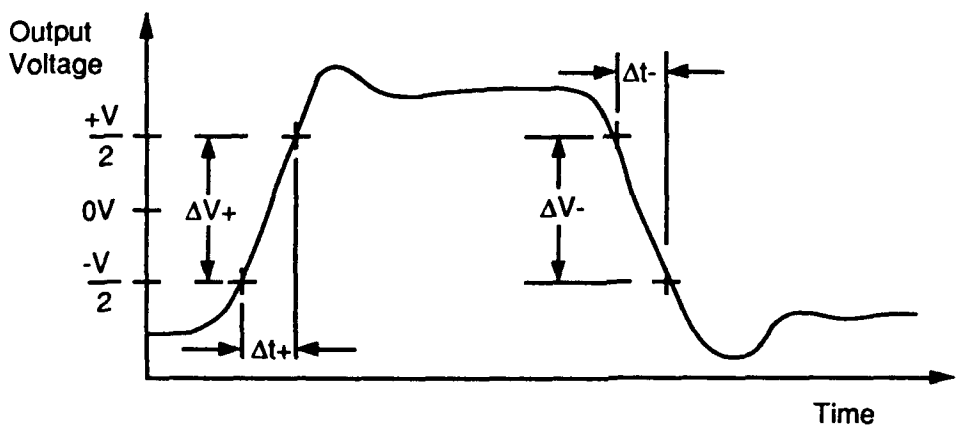
Note: Guardband of +/- 2% used

Settling Time Waveform
For Positive Switching



Note: Guardband of +/- 2% used

Settling Time Waveform
For Negative Switching



$SR(+) = \Delta V+/\Delta t+$ $SR(-) = \Delta V-/\Delta t-$

Slew Rate Waveform

Figure 2. Analog Multiplier Transient Response Waveforms

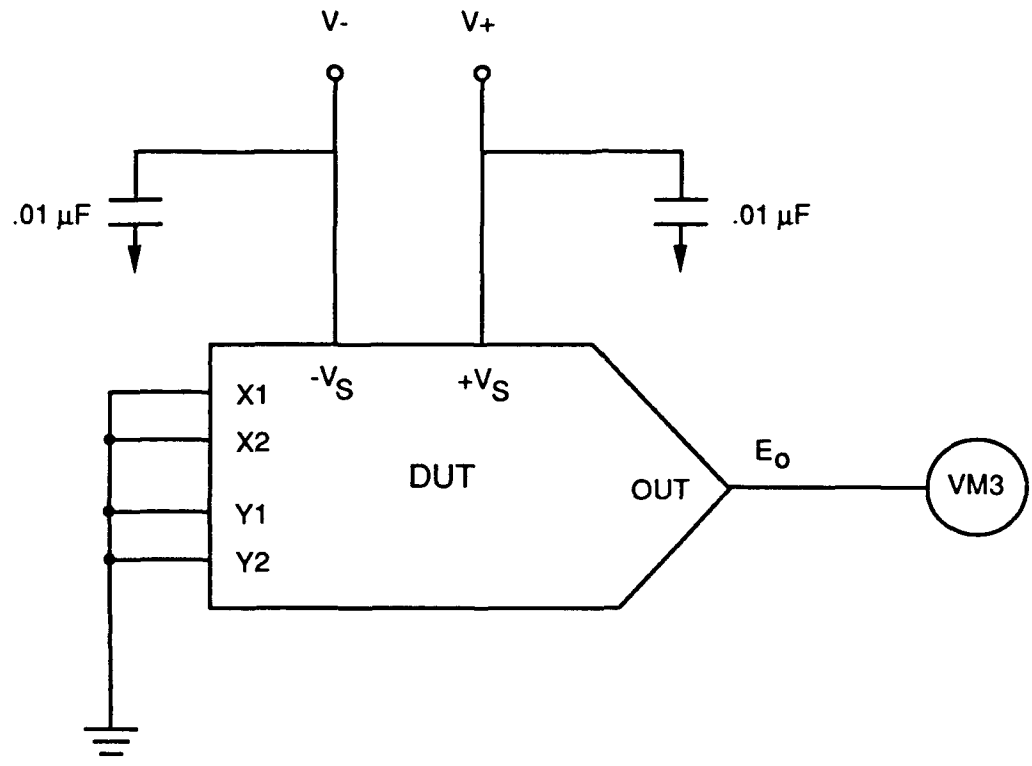


Figure 3. Analog Multiplier Noise Test Circuit

APPENDIX B - Bibliography

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